



SINGLE-CHIP USB to UART DATA TRANSFER

- Integrated USB Transceiver; No External Resistors Required
- Integrated Clock; No External Crystal Required
- Integrated 512-Byte EEPROM for Vendor ID, Product ID, Serial Number, Power Descriptor, Release Number and Product Description Strings
- On-Chip Power-On Reset Circuit
- On-Chip Voltage Regulator: 3.3V Output

USB FUNCTION CONTROLLER

- USB Specification 2.0 Compliant; Full Speed (12 Mbps)
- USB suspend states supported via SUSPEND pins

ASYNCHRONOUS SERIAL DATA BUS (UART)

- All Handshaking and Modem Interface Signals
- Data Formats Supported:
  - Data Bits: 8
  - Stop Bits: 1, 2
  - Parity: Odd, Even, No Parity
- Baud Rates: 300bps to 921.6kbps
- 512 Byte Receive Buffer; 512 Byte Transmit Buffer
- Hardware or X-On / X-Off Handshaking Supported
- Event Character and Line Break Condition Support

VIRTUAL COM PORT DEVICE DRIVERS

- Works with Existing COM Port PC Applications
  - Royalty-Free Distribution License
  - Windows 98/Me/2000/XP
  - MAC OS-9
  - MAC OS-X
  - Windows CE \*
  - Linux 2.40 and greater \*
- \*(Contact factory for availability)

EXAMPLE APPLICATIONS

- Upgrade of RS-232 Legacy Devices to USB
- Cellular Phone USB Interface Cable
- PDA USB Interface Cable
- USB to RS-232 Serial Adapter

SUPPLY VOLTAGE

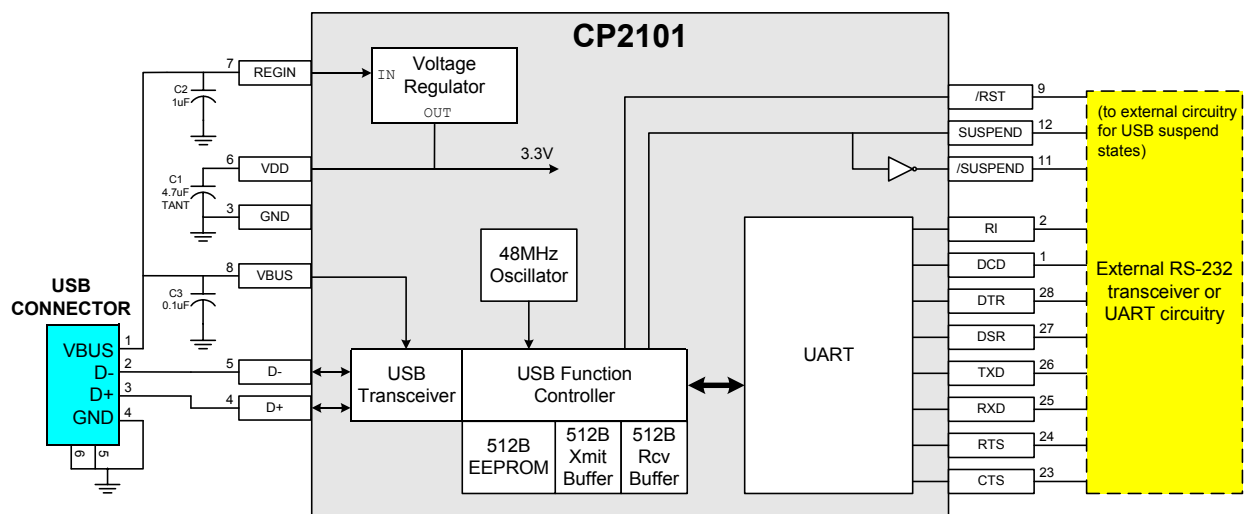
- Self-powered: 3.0V to 3.6V
- USB Bus Powered: 4.0V to 5.25V

PACKAGE

- 28-pin MLP (5mm X 5mm)

TEMPERATURE RANGE: -40°C TO +85°C

Example Circuit Diagram





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*Notes*



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*Notes*



## 1. SYSTEM OVERVIEW

The CP2101 is a highly-integrated USB-to-UART Bridge Controller providing a simple solution for updating RS232 designs to USB using a minimum of components and PCB space. The CP2101 includes a USB 2.0 full-speed function controller, USB transceiver, oscillator, EEPROM and asynchronous serial data bus (UART) with full modem control signals in a compact 5mm X 5mm MLP-28 package. No other external USB components are required.

The on-chip EEPROM may be used to customize the USB Vendor ID, Product ID, Product Description String, Power Descriptor, Device Release Number and Device Serial Number as desired for OEM applications. The EEPROM is programmed on-board via the USB allowing the programming step to be easily integrated into the product manufacturing and testing process.

Royalty-free Virtual COM Port (VCP) device drivers provided by Cygnal allow a CP2101-based product to appear as a COM port to PC applications. The CP2101 UART interface implements all RS232 signals, including control and handshaking signals, so existing system firmware does not need to be modified. In many existing RS232 designs, all that is required to update the design from RS232 to USB is to replace the RS232 level-translator with the CP2101.

An evaluation kit for the CP2101 (Part Number: CP2101EK) is available. It includes a CP2101-based USB-to-UART/RS232 evaluation board, a complete set of VCP device drivers, USB and RS232 cables and full documentation. Contact any of Cygnal's sales representatives or go to [www.cygnal.com](http://www.cygnal.com) to order the CP2101 Evaluation Kit.

## 2. ABSOLUTE MAXIMUM RATINGS

Table 2.1. Absolute Maximum Ratings\*

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Ambient temperature under bias		-55		125	°C
Storage Temperature		-65		150	°C
Voltage on any I/O Pin or /RST with respect to GND		-0.3		5.8	V
Voltage on VDD with respect to GND		-0.3		4.2	V
Maximum Total current through VDD and GND				500	mA
Maximum output current sunk by /RST or any I/O pin				100	mA

\*Note: stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.



### 3. GLOBAL DC ELECTRICAL CHARACTERISTICS

**Table 3.1. Global DC Electrical Characteristics**

-40°C to +85°C unless otherwise specified

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Digital Supply Voltage		3.0	3.3	3.6	V
Digital Supply Current with USB active	VDD=3.3V		TBD		mA
Specified Operating Temperature Range		-40		+85	°C

### 4. PINOUT AND PACKAGE DEFINITIONS

**Table 4.1. Pin Definitions for the CP2101**

Name	Pin Number	Type	Description
VDD	6	Power In	3.0-3.6 V Power Supply Voltage Input.
		Power Out	3.3 V Voltage Regulator Output. See <a href="#">Section 9</a> .
GND	3		Ground
/RST	9	D I/O	Device Reset. Open-drain output of internal POR or VDD monitor. An external source can initiate a system reset by driving this pin low for at least 15 $\mu$ s.
REGIN	7	Power In	5 V Regulator Input. This pin is the input to the on-chip voltage regulator.
VBUS	8	D In	VBUS Sense Input. This pin should be connected to the VBUS signal of a USB network. A 5 V signal on this pin indicates a USB network connection.
D+	4	D I/O	USB D+
D-	5	D I/O	USB D-
TXD	26	D Out	Asynchronous data output (UART Transmit)
RXD	25	D In	Asynchronous data input (UART Receive)
CTS	23	D In	Clear To Send control input (active low)
RTS	24	D Out	Ready to Send control output (active low)
DSR	27	D in	Data Set Ready control output (active low)
DTR	28	D Out	Data Terminal Ready control output (active low)
DCD	1	D In	Data Carrier Detect control input (active low)
RI	2	D In	Ring Indicator control input (active low)



Table 4.1. Pin Definitions for the CP2101

Name	Pin Number	Type	Description
SUSPEND	12	D Out	This pin is driven high when the CP2101 enters the USB Suspend state.
/SUSPEND	11	D Out	This pin is driven low when the CP2101 enters the USB Suspend state.
NC	10, 13-22		These pins should be left unconnected or tied to VDD.

Figure 4.1. MLP-28 Pinout Diagram (Top View)

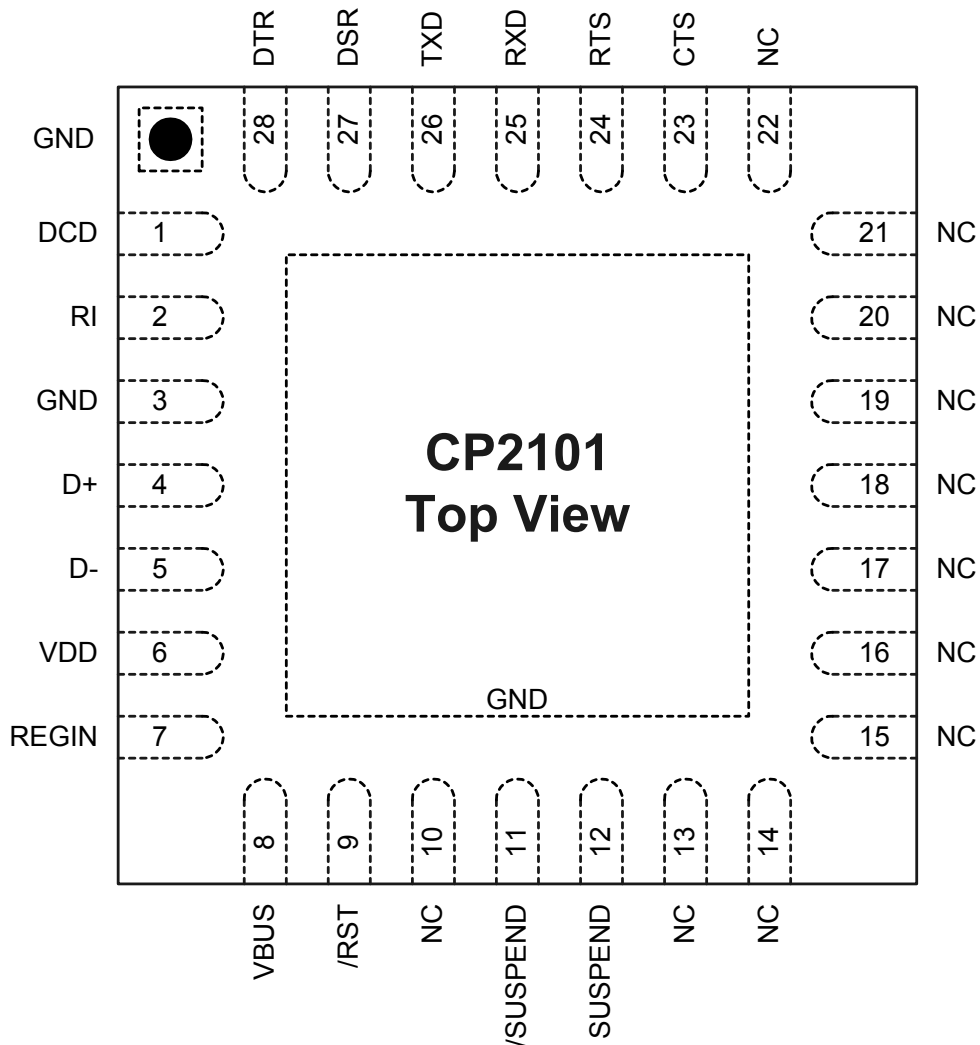




Figure 4.2. MLP-28 Package Drawing

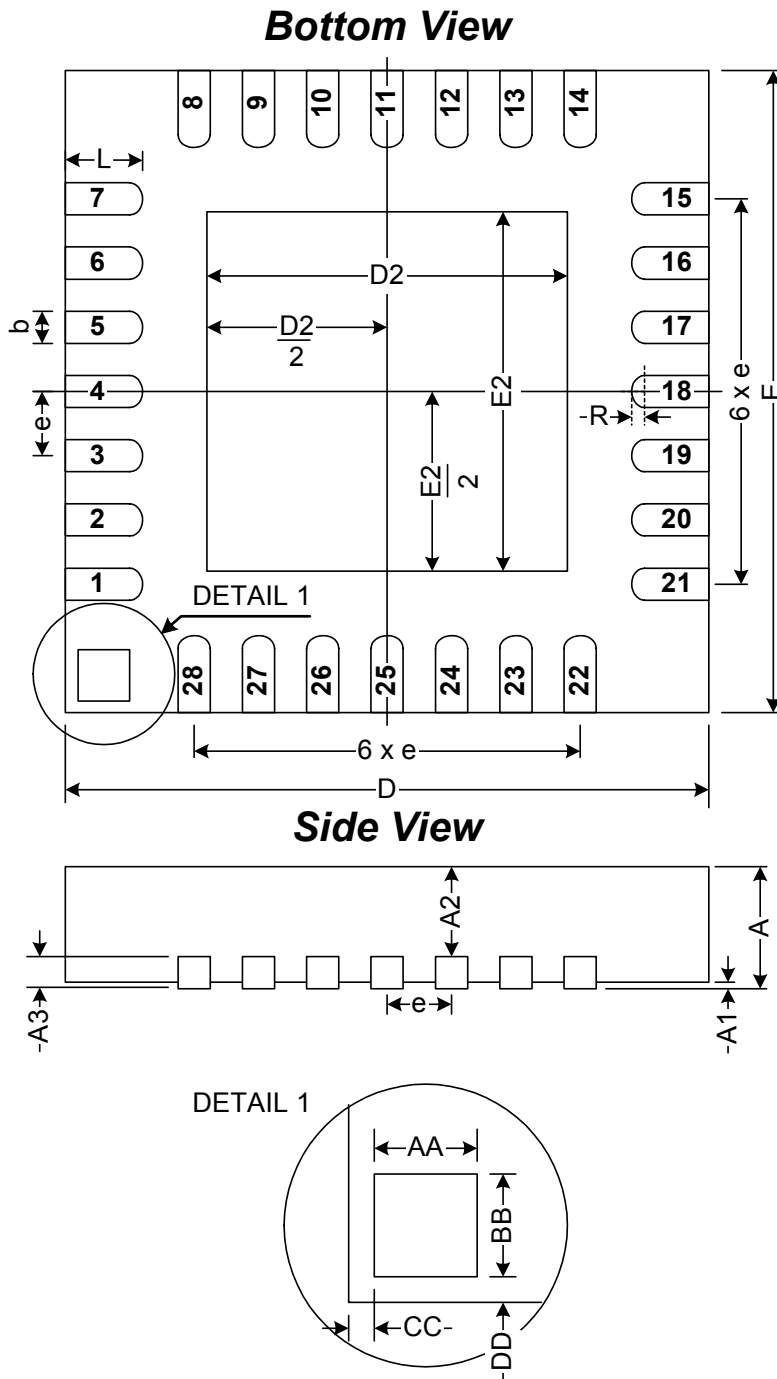


Table 4.2. MLP-28 Package Dimensions

	MM		
	MIN	TYP	MAX
A	0.80	0.90	1.00
A1	0	0.02	0.05
A2	0	0.65	1.00
A3	-	0.25	-
b	0.18	0.23	0.30
D	-	5.00	-
D2	2.90	3.15	3.35
E	-	5.00	-
E2	2.90	3.15	3.35
e	-	0.5	-
L	0.45	0.55	0.65
N	-	28	-
ND	-	7	-
NE	-	7	-
R	0.09	-	-
AA	-	0.435	-
BB	-	0.435	-
CC	-	0.18	-
DD	-	0.18	-



Figure 4.3. Typical MLP-28 Landing Diagram

Top View

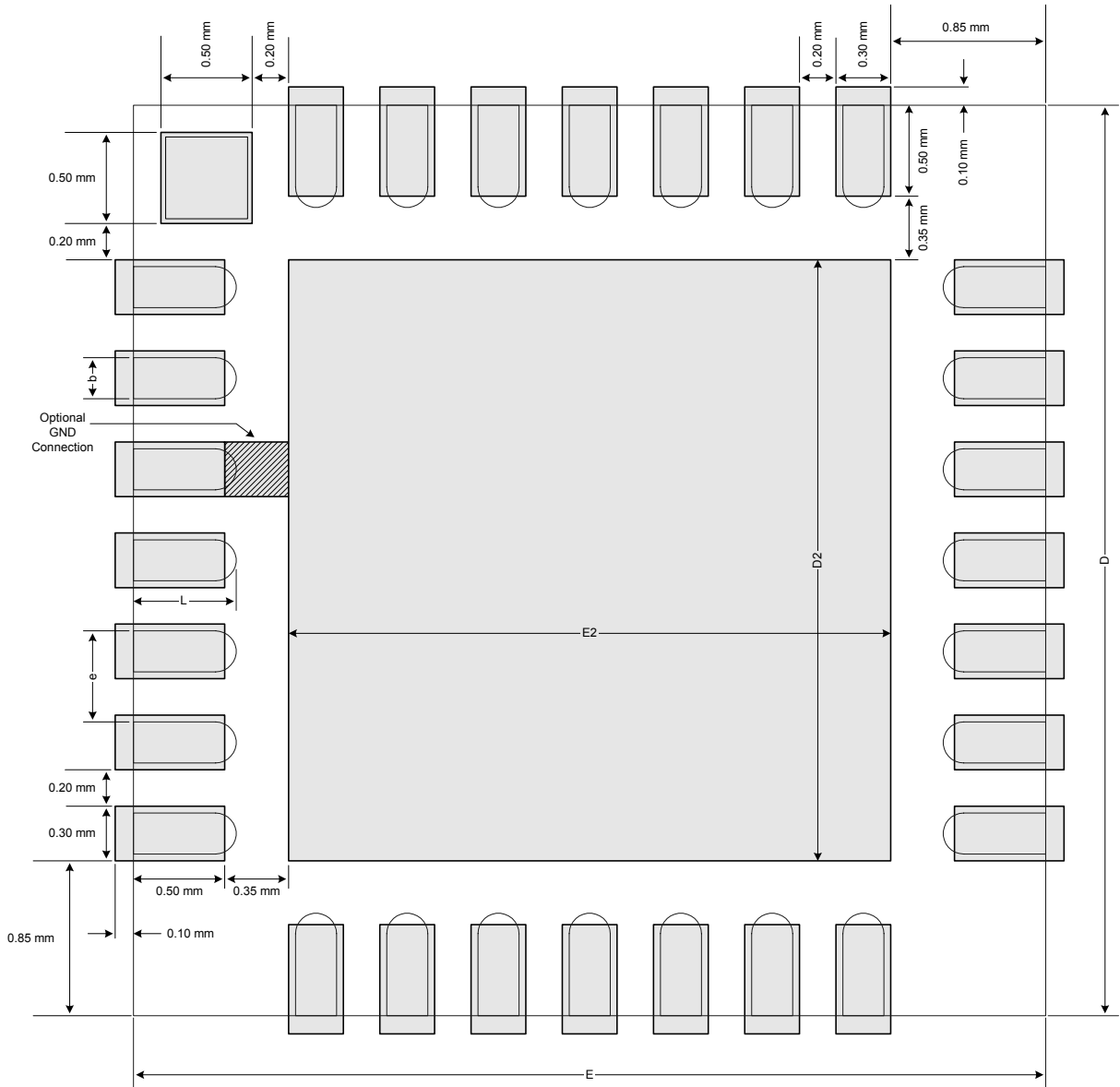
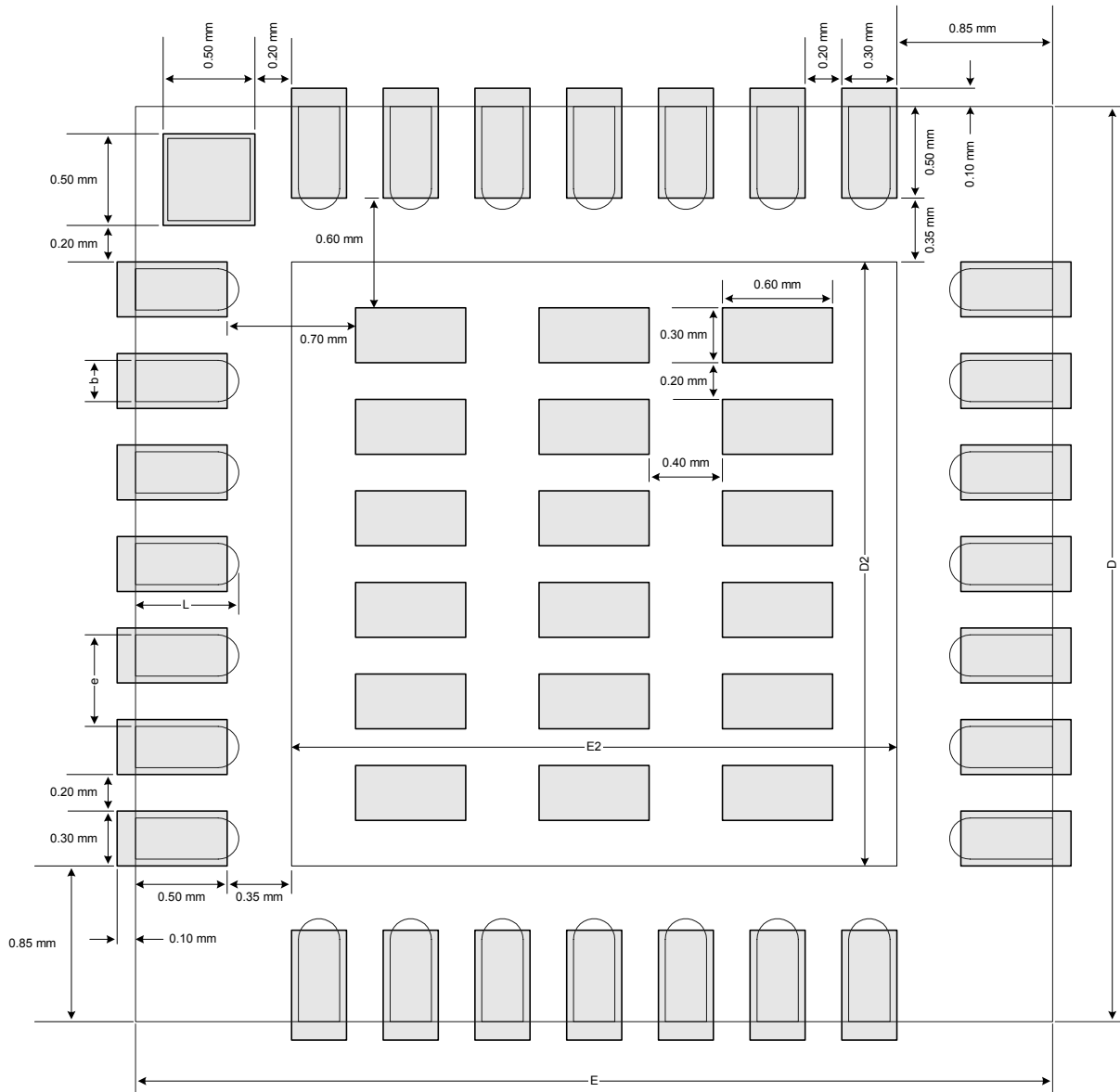


Figure 4.4. Typical MLP-28 Solder Mask

Top View





## 5. USB FUNCTION CONTROLLER AND TRANSCEIVER

The Universal Serial Bus function controller in the CP2101 is a USB 2.0 compliant full-speed device with integrated transceiver and on-chip matching and pull-up resistors. The USB function controller manages all data transfers between the USB and the UART as well as command requests generated by the USB host controller and commands for controlling the function of the UART.

The USB Suspend and Resume signals are supported for power management of both the CP2101 device as well as external circuitry. The CP2101 will enter Suspend mode when Suspend signaling is detected on the bus. On entering Suspend mode, the CP2101 asserts the SUSPEND and /SUSPEND signals. SUSPEND and /SUSPEND are also asserted after a CP2101 reset until device configuration during USB Enumeration is complete

The CP2101 exits the Suspend mode when any of the following occur: (1) Resume signaling is detected or generated, (2) a USB Reset signal is detected, or (3) a device reset occurs. On exit of Suspend mode, the SUSPEND and /SUSPEND signals are de-asserted. Note: both SUSPEND and /SUSPEND temporarily float high during a CP2101 reset. If this behavior is undesirable, a strong pull-down (10K ohms) can be used to ensure /SUSPEND remains low during reset.

## 6. ASYNCHRONOUS SERIAL DATA BUS (UART) INTERFACE

The CP2101 UART interface consists of the TX (transmit) and RX (receive) data signals as well as the RTS, CTS, DSR, DTR, DCD and RI control signals. The UART supports RTS/CTS, DSR/DTR and X-On/X-Off handshaking.

The UART is programmable to support a variety of data formats and baud rates. The data format and baud rate programmed into the UART is set during COM port configuration on the PC. The data formats and baud rates available are listed in Table 6.1.

**Table 6.1. Data Formats and Baud Rates**

Data Bits	8
Stop Bits	1
Parity Type	None, Even, Odd
Baud Rates	300, 600, 1200, 1800, 2400, 4800, 7200, 9600, 14400, 19200, 28800, 38400, 56000, 57600, 115200, 128000, 230400, 460800, 921600



## 7. INTERNAL EEPROM

The CP2101 includes an internal EEPROM which may be used to customize the USB Vendor ID, Product ID, Product Description String, Power Descriptor, Device Release Number and Device Serial Number as desired for OEM applications. Customization of the USB configuration data is optional. If the EEPROM is not programmed with OEM data, the default configuration data shown in Table 6.1 is used. Note, however, a unique serial number is required for OEM applications in which it is possible for multiple CP2101-based devices to be connected to the same PC.

The internal EEPROM is programmed via the USB. This allows the OEM's USB configuration data and serial number to be written to the CP2101 on-board during the manufacturing and testing process. A stand-alone utility for programming the internal EEPROM is available from Cygnal. A library of routines provided in the form of a Windows DLL is also available. This library can be used to integrate the EEPROM programming step into custom software used by the OEM to streamline testing and serial number management during manufacturing. The EEPROM has a typical endurance of 100,000 write cycles with a data retention of 100 years.

**Table 7.1. Default USB Configuration Data**

NAME	VALUE
Vendor ID	10C4h
Product ID	EA60h
Power Descriptor (Attributes)	80h
Power Descriptor (Max. Power)	0Fh
Release Number	0100h
Serial Number	0001 (63 characters maximum)
Product Description String	“CygnaL CP2101 USB to UART Bridge Controller” (126 characters maximum)

## 8. VIRTUAL COM PORT DEVICE DRIVERS

The CP2101 Virtual COM Port (VCP) device drivers allow a CP2101-based device to appear to the PC's application software as an additional COM port (in addition to any existing hardware COM ports). Application software running on the PC accesses the CP2101-based device as it would access a standard hardware COM port. However, actual data transfer between the PC and the CP2101 device is performed over the USB. Therefore, existing COM port applications may be used to transfer data via the USB to the CP2101-based device without modifying the application. Contact Cygnal Integrated Products for the latest list of supported operating systems.

Note: the Cygnal VCP device drivers are required for device operation and are only distributed as part of the CP2101 Evaluation Kit (Part Number: CP2101EK). Contact any of Cygnal's sales representatives or go to [www.cygnal.com](http://www.cygnal.com) to order the CP2101 Evaluation Kit.



## 9. VOLTAGE REGULATOR

The CP2101 is designed to be a USB bus-powered device taking power from the USB VBUS signal. It includes an on-chip 5 V-to-3 V voltage regulator for this purpose. The 3 V output of the voltage regulator appears on the VDD pin allowing external 3 V devices to be powered from the USB. See Table 9.1 for the voltage regulator's electrical specifications.

Note: both the VBUS and RGIN pins of the CP2101 should always be connected to the USB VBUS signal. It is recommended that additional decoupling capacitance (ex. 0.1  $\mu$ F in parallel with 1.0  $\mu$ F) be provided on the RGIN input.

**Table 9.1. Voltage Regulator Electrical Specifications**

VDD = 3.0 V; -40°C to +85°C unless otherwise specified

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range		4.0		5.25	V
Output Voltage	Output Current = 1 to 100 mA	3.0	3.3	3.6	V
VBUS Detection Input Threshold		1.0	1.8	4.0	V
Bias Current			90	TBD	$\mu$ A



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