

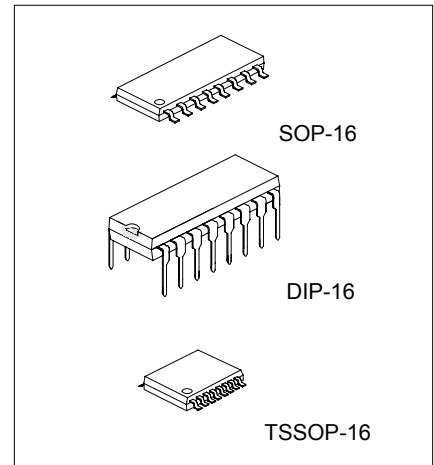
ANALOG MULTIPLEXERS/ DEMULTIPLEXERS

**DESCRIPTION**

The UTC 4053 are Triple SPDT analog multiplexers for application as digitally-controlled analog switches.

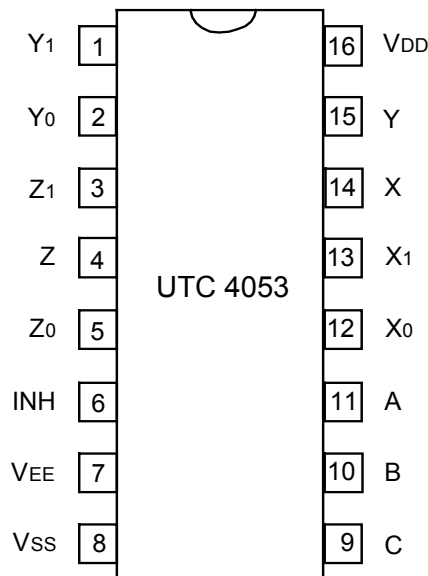
**FEATURES**

- \* Analog Voltage Range ( $V_{DD} - V_{EE}$ ) = 3.0 ~ 18 V  
Note:  $V_{EE}$  must be  $\leq V_{SS}$
- \* Linearized Transfer Characteristics
- \* Pin-to-Pin Replacement for CD4053

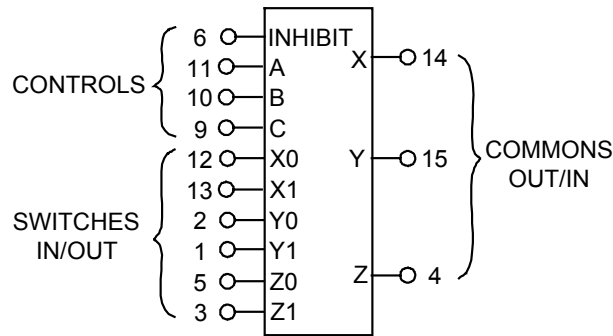


\*Pb-free plating product number: 4053L

**PIN CONFIGURATIONS**



UTC 4053 Triple 2-Channel Analog Multiplexer/Demultiplexer



V<sub>DD</sub> = PIN 16  
 V<sub>SS</sub> = PIN 8  
 V<sub>EE</sub> = PIN 7

Note: Control Inputs referenced to V<sub>SS</sub>, Analog Inputs and Outputs reference to V<sub>EE</sub>. V<sub>EE</sub> must be ≤ V<sub>SS</sub>.

**ABSOLUTE MAXIMUM RATINGS\***

PARAMETER	SYMBOL	RATINGS	UNIT
DC Supply Voltage (Referenced to V <sub>EE</sub> , V <sub>SS</sub> ≥ V <sub>EE</sub> )	V <sub>DD</sub>	-0.5 ~ +18.0	V
Input or Output Voltage (DC or Transient) (Referenced to V <sub>SS</sub> for Control Inputs and V <sub>EE</sub> for Switch I/O)	V <sub>in</sub> , V <sub>out</sub>	-0.5 ~ V <sub>DD</sub> + 0.5	V
Input Current (DC or Transient), per Control Pin	I <sub>in</sub>	±10	mA
Switch Through Current	I <sub>SW</sub>	±25	mA
Power Dissipation. Per Package**	P <sub>D</sub>	500	mW
Storage Temperature	T <sub>stg</sub>	-65 ~ +150	°C
Lead Temperature (8 - Second Soldering)	T <sub>Lead</sub>	260	°C

\* Maximum Ratings are those values beyond which damage to the device may occur.

\*\* Temperature Derating: "DIP and SOP" Packages: - 7.0 mW/°C From 65°C ~ 125°C

**ELECTRICAL CHARACTERISTICS**

(T<sub>a</sub>=25°C, unless otherwise indicated.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP#	MAX	UNIT
<b>SUPPLY REQUIREMENTS (Voltages Referenced to V<sub>EE</sub>)</b>						
Power Supply Voltage Range	V <sub>DD</sub>	V <sub>DD</sub> - 3.0 ≥ V <sub>SS</sub> ≥ V <sub>EE</sub>	3.0		18	V
Quiescent Current per Package	I <sub>DD</sub>	Control Inputs: V <sub>in</sub> = V <sub>SS</sub> or V <sub>DD</sub> Switch I/O: V <sub>EE</sub> ≤ V <sub>I/O</sub> ≤ V <sub>DD</sub> , and ΔV <sub>switch</sub> ≤ 500mV* V <sub>DD</sub> =5.0V V <sub>DD</sub> =10V V <sub>DD</sub> =15V		0.005 0.010 0.015	5.0 10 20	μA
Total Supply Current (Dynamic Plus Quiescent, Per Package)	I <sub>D(AV)</sub>	T <sub>a</sub> =25°C only (The channel component, (V <sub>in</sub> - V <sub>out</sub> )/R <sub>on</sub> , is not included.) V <sub>DD</sub> =5.0V V <sub>DD</sub> =10V V <sub>DD</sub> =15V		(0.07 μA/kHz) f + I <sub>DD</sub> Typical (0.20 μA/kHz) f + I <sub>DD</sub> (0.36 μA/kHz) f + I <sub>DD</sub>		μA

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP#	MAX	UNIT
<b>CONTROL INPUTS – INHIBIT A, B, C (Voltages Referenced to V<sub>SS</sub>)</b>						
Low – Level Input Voltage	V <sub>IL</sub>	R <sub>on</sub> = per spec, I <sub>off</sub> = per spec V <sub>DD</sub> =5.0V V <sub>DD</sub> =10V V <sub>DD</sub> =15V		2.25 4.50 6.75	1.5 3.0 4.0	V
High – Level Input Voltage	V <sub>IH</sub>	R <sub>on</sub> = per spec, I <sub>off</sub> = per spec V <sub>DD</sub> =5.0V V <sub>DD</sub> =10V V <sub>DD</sub> =15V	3.5 7.0 11	2.75 5.50 8.25		V
Input Leakage Current	I <sub>in</sub>	V <sub>in</sub> = 0 or V <sub>DD</sub> , V <sub>DD</sub> =15V		±0.00001	±0.1	µA
Input Capacitance	C <sub>in</sub>			5.0	7.5	pF
<b>SWITCHES IN/OUT AND COMMONS OUT/IN -- X, Y, Z (Voltages Referenced to V<sub>EE</sub>)</b>						
Recommended Peak-to-Peak Voltage Into or Out of the Switch	V <sub>I/O</sub>	Channel On or Off	0		V <sub>DD</sub>	V <sub>PP</sub>
Recommended Static or Dynamic Voltage Across the Switch** (Figure 3)	ΔV <sub>switch</sub>	Channel On	0		600	mV
Output Offset Voltage	V <sub>OO</sub>	V <sub>in</sub> = 0V, No Load		10		µV
ON Resistance	R <sub>on</sub>	ΔV <sub>switch</sub> ≤ 500mV* V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> (Control), and V <sub>in</sub> = 0 to V <sub>DD</sub> (Switch) V <sub>DD</sub> =5.0V V <sub>DD</sub> =10V V <sub>DD</sub> =15V		250 120 80	1050 500 280	Ω
Δ ON Resistance Between Any Two Channels in the Same Package	ΔR <sub>on</sub>	V <sub>DD</sub> =5.0V V <sub>DD</sub> =10V V <sub>DD</sub> =15V		25 10 10	70 50 45	Ω
Off-Channel Leakage Current (Figure 8)	I <sub>off</sub>	V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> (Control) Channel to Channel or Any One Channel, V <sub>DD</sub> =15V		±0.05	±100	nA
Capacitance, Switch I/O	C <sub>I/O</sub>	Inhibit = V <sub>DD</sub>		10		pF
Capacitance, Common O/I	C <sub>O/I</sub>	Inhibit = V <sub>DD</sub>		17		pF
Capacitance, Feedthrough (Channel Off)	C <sub>I/O</sub>	Pins Not Adjacent Pins Adjacent		0.15 0.47		pF

#Data labeled "Typ" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.

\* For voltage drops across the switch (ΔV<sub>switch</sub>) > 600 mV (> 300 mV at high temperature), excessive V<sub>DD</sub> current may be drawn, i.e. the current out of the switch may contain both V<sub>DD</sub> and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See second page of this data sheet.)

**ELECTRICAL CHARACTERISTICS\***

( $C_L = 50\text{pF}$ ,  $T_a = 25^\circ\text{C}$ ,  $V_{EE} \leq V_{SS}$ , unless otherwise indicated.)

PARAMETER	SYMBOL	$V_{DD} - V_{EE}$ Vdc	TEST CONDITIONS	MIN	TYP#	MAX	UNIT
Propagation Delay Times (Figure 4) Switch Input to Switch Output ( $R_L = 10\text{ k}\Omega$ )	$t_{PLH}$ , $t_{PHL}$	5.0	$t_{PLH}$ , $t_{PHL} = (0.17\text{ ns/pF}) C_L + 16.5\text{ ns}$		25	65	ns
		10	$t_{PLH}$ , $t_{PHL} = (0.08\text{ ns/pF}) C_L + 4.0\text{ ns}$		8.0	20	
		15	$t_{PLH}$ , $t_{PHL} = (0.06\text{ ns/pF}) C_L + 3.0\text{ ns}$		6.0	15	
Inhibit to Output	$t_{PHZ}$ , $t_{PLZ}$ $t_{PZH}$ , $t_{PZL}$	5.0	$(R_L = 10\text{ k}\Omega, V_{EE} = V_{SS})$ Output "1" or "0" to High Impedance, or High Impedance to "1" or "0" Level		275	550	ns
		10		140	280		
		15		110	220		
Control Input to Output	$t_{PLH}$ , $t_{PHL}$	5.0	$R_L = 10\text{ k}\Omega, V_{EE} = V_{SS}$		300	600	ns
		10		120	240		
		15		80	160		
Second Harmonic Distortion		10	$R_L = 10\text{ k}\Omega, f = 1\text{ kHz}, V_{in} = 5\text{ V}_{PP}$		0.07		%
Bandwidth (Figure 5)	BW	10	$R_L = 1\text{ k}\Omega, V_{in} = 1/2 (V_{DD} - V_{EE})\text{ p-p}$ , $C_L = 50\text{ pF}, 20\text{ Log}(V_{out}/V_{in}) = -3\text{ dB}$		17		MHz
Off Channel Feedthrough Attenuation (Figure 5)		10	$R_L = 1\text{ k}\Omega, V_{in} = 1/2 (V_{DD} - V_{EE})\text{ p-p}$ $f_{in} = 55\text{ MHz}$		-50		dB
Channel Separation (Figure 6)		10	$R_L = 1\text{ k}\Omega, V_{in} = 1/2 (V_{DD} - V_{EE})\text{ p-p}$ $f_{in} = 3.0\text{ MHz}$		-50		dB
Crosstalk, Control Input to Common O/I (Figure 7)		10	$R_1 = 1\text{ k}\Omega, R_L = 10\text{ k}\Omega$ Control $t_{TLH} = t_{THL} = 20\text{ ns}, \text{Inhibit} = V_{SS}$		75		mV

\* The formulas given are for the typical characteristics only at  $25^\circ\text{C}$ .

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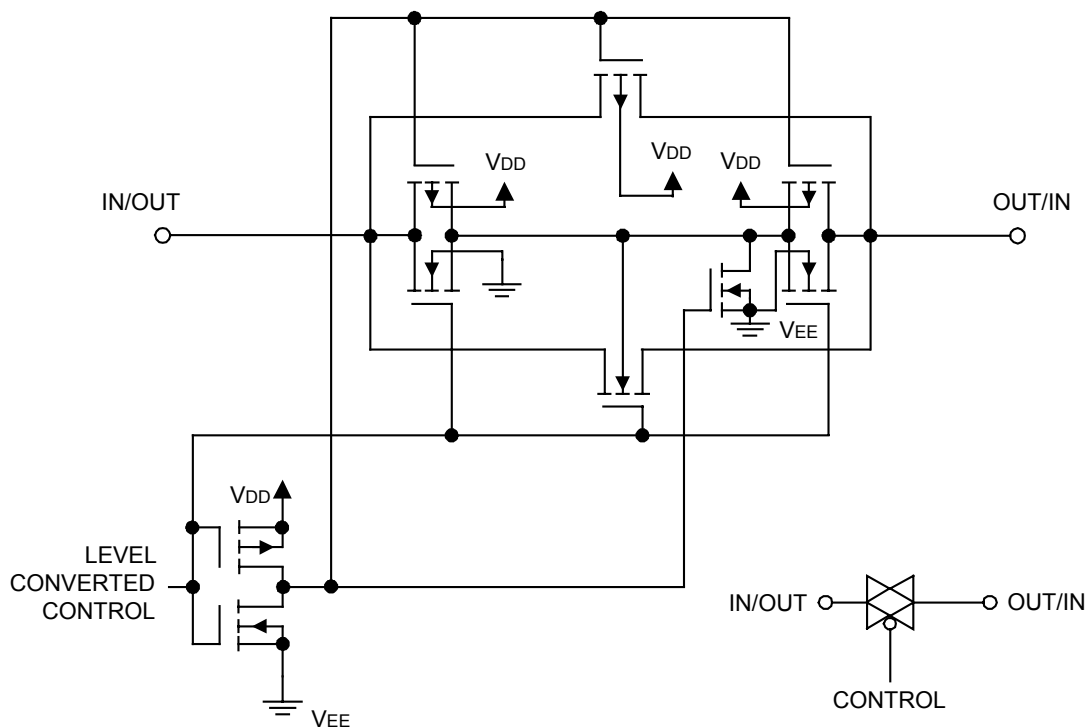


Figure 1. Switch Circuit Schematic

TRUTH TABLE

Control Inputs			ON Switches			
Inhibit	Select			UTC 4053		
	C	B	A	Z0	Y0	X0
0	0	0	0	Z0	Y0	X0
0	0	0	1	Z0	Y0	X1
0	0	1	0	Z0	Y1	X0
0	0	1	1	Z0	Y1	X1
0	1	0	0	Z1	Y0	X0
0	1	0	1	Z1	Y0	X1
0	1	1	0	Z1	Y1	X0
0	1	1	1	Z1	Y1	X1
1	x	x	x	None		

x = Don't Care

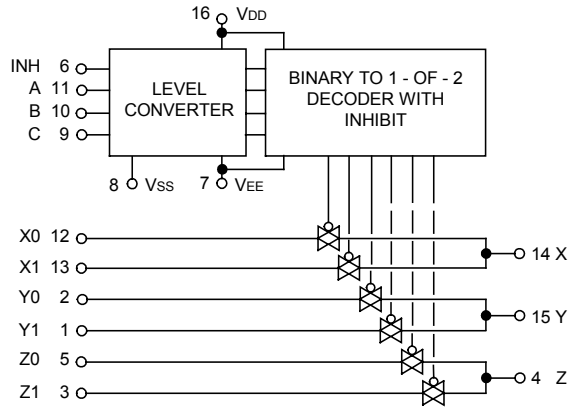
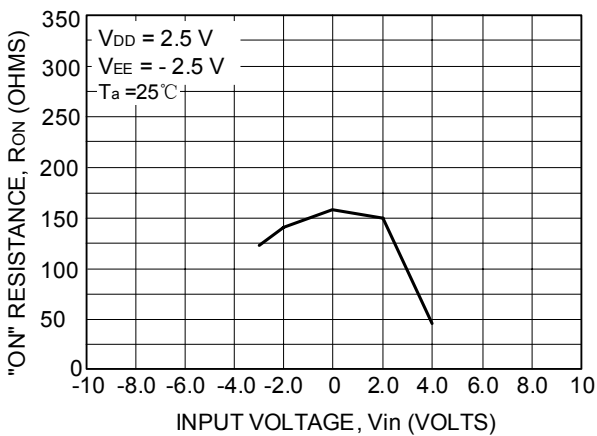
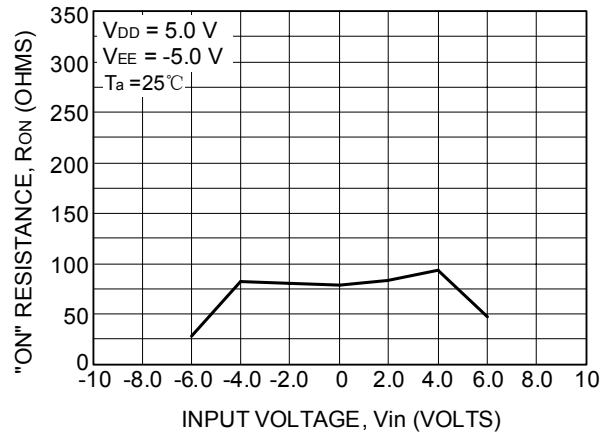
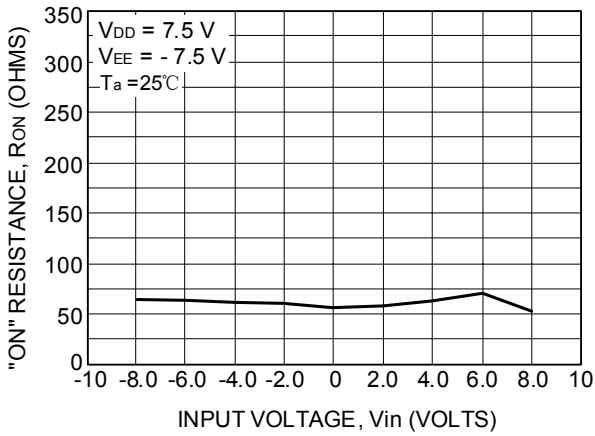


Figure 2. UTC 4053 Functional Diagram



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