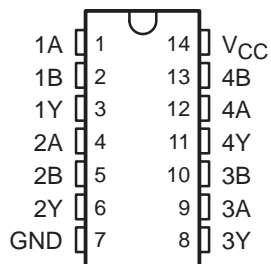


# SN54ACT32, SN74ACT32 QUADRUPLE 2-INPUT POSITIVE-OR GATES

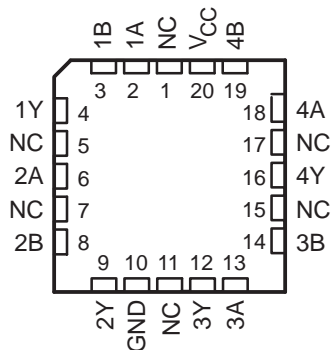
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- 4.5-V to 5.5-V  $V_{CC}$  Operation
- Inputs Accept Voltages to 5.5 V
- Max  $t_{pd}$  of 10 ns at 5 V
- Inputs Are TTL-Voltage Compatible

SN54ACT32 . . . J OR W PACKAGE  
SN74ACT32 . . . D, DB, N, NS, OR PW PACKAGE  
(TOP VIEW)



SN54ACT32 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## description/ordering information

The 'ACT32 devices are quadruple 2-input positive-OR gates. The devices perform the Boolean function  $Y = A + B$  or  $Y = \overline{A} \cdot \overline{B}$  in positive logic.

## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube	SN74ACT32N	SN74ACT32N
	SOIC – D	Tube	SN74ACT32D	
		Tape and reel	SN74ACT32DR	ACT32
	SOP – NS	Tape and reel	SN74ACT32NSR	ACT32
	SSOP – DB	Tape and reel	SN74ACT32DBR	AD32
	TSSOP – PW	Tube	SN74ACT32PW	AD32
Tape and reel		SN74ACT32PWR		
–55°C to 125°C	CDIP – J	Tube	SNJ54ACT32J	SNJ54ACT32J
	CFP – W	Tube	SNJ54ACT32W	SNJ54ACT32W
	LCCC – FK	Tube	SNJ54ACT32FK	SNJ54ACT32FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

FUNCTION TABLE  
(each gate)

INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L



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 **TEXAS  
INSTRUMENTS**

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# SN54ACT32, SN74ACT32 QUADRUPLE 2-INPUT POSITIVE-OR GATES

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logic diagram, each gate (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Note 1) .....	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) .....	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	$\pm 20$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	$\pm 50$ mA
Continuous current through $V_{CC}$ or GND .....	$\pm 200$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package .....	86°C/W
DB package .....	96°C/W
N package .....	80°C/W
NS package .....	76°C/W
PW package .....	113°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 3)

	SN54ACT32		SN74ACT32		UNIT
	MIN	MAX	MIN	MAX	
$V_{CC}$ Supply voltage	4.5	5.5	4.5	5.5	V
$V_{IH}$ High-level input voltage	2		2		V
$V_{IL}$ Low-level input voltage		0.8		0.8	V
$V_I$ Input voltage	0	$V_{CC}$	0	$V_{CC}$	V
$V_O$ Output voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$ High-level output current		-24		-24	mA
$I_{OL}$ Low-level output current		24		24	mA
$\Delta t/\Delta v$ Input transition rise or fall rate		8		8	ns/V
$T_A$ Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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# SN54ACT32, SN74ACT32 QUADRUPLE 2-INPUT POSITIVE-OR GATES

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54ACT32		SN74ACT32		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	4.5 V	4.4			4.4		4.4	V	
		5.5 V	5.4			5.4		5.4		
	I <sub>OH</sub> = -24 mA	4.5 V	3.86			3.7		3.76		
		5.5 V	4.86			4.7		4.76		
		5.5 V				3.86				
I <sub>OH</sub> = -75 mA†	5.5 V						3.85			
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	4.5 V		0.001	0.1		0.1	0.1	V	
		5.5 V		0.001	0.1		0.1	0.1		
	I <sub>OL</sub> = 24 mA	5.5 V			0.36		0.5	0.44		
		5.5 V			0.36		0.5	0.44		
	I <sub>OL</sub> = 50 mA†	5.5 V					1.65			
I <sub>OL</sub> = 75 mA†	5.5 V						1.65			
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V			±0.1		±1	±1	μA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			2		40	20	μA	
ΔI <sub>CC</sub> ‡	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	5.5 V		0.6			1.6	1.5	mA	
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		2.6					pF	

† Not more than one output should be tested at a time, and the duration of the test should not exceed 2 ms.

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V<sub>CC</sub>.

switching characteristics over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T <sub>A</sub> = 25°C			SN54ACT32		SN74ACT32		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A or B	Y	1	6.5	9			1	10	ns
t <sub>PHL</sub>			1	6.5	9			1	10	

operating characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub> Power dissipation capacitance	C <sub>L</sub> = 50 pF, f = 1 MHz	40	pF

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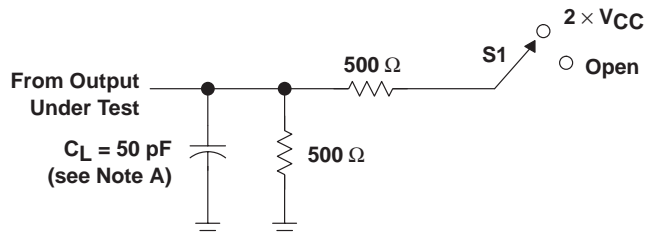
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# SN54ACT32, SN74ACT32 QUADRUPLE 2-INPUT POSITIVE-OR GATES

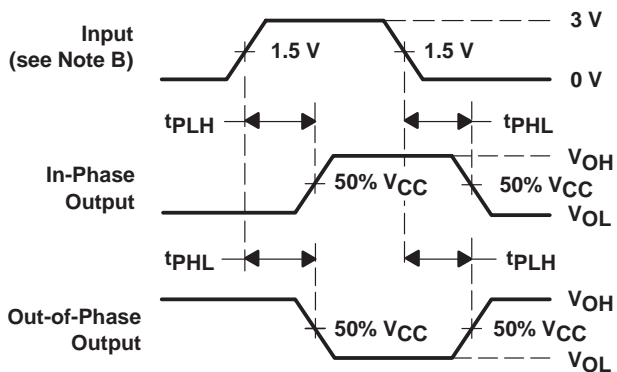
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## PARAMETER MEASUREMENT INFORMATION

TEST	S1
$t_{PLH}/t_{PHL}$	Open



LOAD CIRCUIT



VOLTAGE WAVEFORMS

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74ACT32D	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74ACT32DBLE	OBSOLETE	SSOP	DB	14		None	Call TI	Call TI
SN74ACT32DBR	ACTIVE	SSOP	DB	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74ACT32DR	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74ACT32N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74ACT32NSR	ACTIVE	SO	NS	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74ACT32PW	ACTIVE	TSSOP	PW	14	90	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74ACT32PWLE	OBSOLETE	TSSOP	PW	14		None	Call TI	Call TI
SN74ACT32PWR	ACTIVE	TSSOP	PW	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**None:** Not yet available Lead (Pb-Free).

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-012 variation AB.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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