

AD7750–SPECIFICATIONS

($V_{DD} = 5\text{ V} \pm 5\%$, $AGND = 0\text{ V}$, $DGND = 0\text{ V}$, $REFIN = +2.5\text{ V}$, $CLKIN = 3.58\text{ MHz}$
 T_{MIN} to $T_{MAX} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $ACDC = \text{Logic High}$)

Parameter	A Version –40°C to +85°C	Units	Test Conditions/Comments
ACCURACY			
Measurement Error ¹			Channel 2 with Full-Scale Signal
Gain = 1	0.2	% Reading max	Measured Over a Dynamic Range on Channel 1 of 500:1
	0.3	% Reading max	Measured Over a Dynamic Range on Channel 1 of 1000:1
Gain = 16	0.2	% Reading max	Measured Over a Dynamic Range on Channel 1 of 500:1
	0.4	% Reading max	Measured Over a Dynamic Range on Channel 1 of 1000:1
Phase Error Between Channels			CLKIN = 3.58 MHz, Line Frequency = 50 Hz
Phase Lead 40° (PF = +0.8)	±0.2	Degrees (°) max	HPF Filter On, ACDC = 1
Phase Lag 60° (PF = –0.5)	±0.2	Degrees (°) max	HPF Filter On, ACDC = 1
Feedthrough Between Channels			HPF Filter On, ACDC = 1, Mode 3, Channel 1 = 0 V
Output Frequency Variation (F_{OUT})	0.0005	% Full-Scale max	Channel 2 = 500 mV rms at 50 Hz
Power Supply Rejection			HPF Filter On, ACDC = 1, Mode 3, Channel 1 = 0 V
Output Frequency Variation (F_{OUT})	0.03	% Full-Scale max	Channel 2 = 500 mV rms, Power Supply Ripple 250 mV at 50 Hz. See Figures 1 and 3.
ANALOG INPUTS			
Maximum Signal Levels	±1	V max	On Any Input, V_{1+} , V_{1-} , V_{2+} and V_{2-} . See Analog Inputs.
Input Impedance (DC)	400	kΩ min	CLKIN = 3.58 MHz
Bandwidth	3.5	kHz typ	CLKIN = 3.58 MHz, CLKIN/1024
Offset Error	±10	mV typ	
Gain Error	±4	% Full-Scale typ	
Gain Error Match	±0.3	% Full-Scale typ	
REFERENCE INPUT			
REF _{IN} Input Voltage Range	2.7	V max	2.5 V + 8%
	2.3	V min	2.5 V – 8%
Input Impedance	50	kΩ min	
ON-CHIP REFERENCE			
Reference Error	±200	mV max	Nominal 2.5 V
Temperature Coefficient	55	ppm/°C typ	
CLKIN			
Input Clock Frequency	4.5	MHz max	
	2	MHz min	
LOGIC INPUTS			
FS, S1, S2, ACDC and G1			
Input High Voltage, V_{INH}	2.4	V min	$V_{DD} = 5\text{ V} \pm 5\%$
Input Low Voltage, V_{INL}	0.8	V max	$V_{DD} = 5\text{ V} \pm 5\%$
Input Current, I_{IN}	±10	μA max	Typically 10 nA, $V_{IN} = 0\text{ V}$ to V_{DD}
Input Capacitance, C_{IN}	10	pF max	
CLKIN			
Input High Voltage, V_{INH}	4	V min	
Input Low Voltage, V_{INL}	0.4	V max	
LOGIC OUTPUTS²			
F1 and F2			
Output High Voltage, V_{OH}	4.3	V min	$I_{SOURCE} = 8\text{ mA}$ $V_{DD} = 5\text{ V}$
Output Low Voltage, V_{OL}	0.5	V max	$I_{SINK} = 8\text{ mA}$ $V_{DD} = 5\text{ V}$
F_{OUT} and REVP			
Output High Voltage, V_{OH}	4	V min	$I_{SOURCE} = 1\text{ mA}$ $V_{DD} = 5\text{ V} \pm 5\%$
Output Low Voltage, V_{OL}	0.4	V max	$I_{SINK} = 200\text{ μA}$ $V_{DD} = 5\text{ V} \pm 5\%$
High Impedance Leakage Current	±10	μA max	
High Impedance Capacitance	15	pF max	

Parameter	A Version -40°C to +85°C	Units	Test Conditions/Comments
POWER SUPPLY			For Specified Performance, Digital Input @ AGND or V _{DD}
V _{DD}	4.75	V min	5 V - 5%
	5.25	V max	5 V + 5%
I _{DD}	5.5	mA max	Typically 3.5 mA

NOTES

¹See plots in Typical Performance Graphs.²External current amplification/drive should be used if higher current source and sink capabilities are required, e.g., bipolar transistor.

All specifications subject to change without notice.

TIMING CHARACTERISTICS^{1, 2} (V_{DD} = 5 V, AGND = 0 V, DVDD = 0 V, REFIN = REFOUT. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	A Version	Units	Test Conditions/Comments
t ₁ ³	275	ms	F1 and F2 Pulsewidth (Logic Low)
t ₂	See Table I	s	Output Pulse Period. See Table I to Determine the Output Frequency
t ₃	t ₂ /2	s	Time Between F1 Falling Edge and F2 Falling Edge
t ₄ ³	90	ms	F _{OUT} Pulsewidth (Logic High)
t ₅	See Table I	s	F _{OUT} Pulse Period. See Table I to Determine the Output Frequency
t ₆	CLKIN/4	s	Minimum Time Between F1 and F2 Pulse

NOTES

¹Sample tested during initial release and after any redesign or process change that may affect this parameter.²See Figure 18.³The pulsewidths of F1, F2 and F_{OUT} are not fixed for higher output frequencies. See the Digital-to-Frequency Converter (DTF) section for an explanation.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*(T_A = +25°C unless otherwise noted)

V _{DD} to AGND	-0.3 V to +7 V
V _{DD} to DGND	-0.3 V to +7 V
Analog Input Voltage to AGND	
V ₁₊ , V ₁₋ , V ₂₊ and V ₂₋	-6 V to +6 V
Reference Input Voltage to AGND	-0.3 V to V _{DD} + 0.3 V
Digital Input Voltage to DGND	-0.3 V to V _{DD} + 0.3 V
Digital Output Voltage to DGND	-0.3 V to V _{DD} + 0.3 V
Operating Temperature Range	
Commercial (A Version)	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	+150°C

20-Lead SOIC Package, Power Dissipation	450 mW
θ _{JA} Thermal Impedance	74°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	+215°C
Infrared (15 sec)	+220°C
20-Lead Plastic DIP, Power Dissipation	450 mW
θ _{JA} Thermal Impedance	102°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	+215°C
Infrared (15 sec)	+220°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Options
AD7750AN	-40°C to +85°C	20-Lead Plastic DIP	N-20
AD7750AR	-40°C to +85°C	20-Lead Wide Body SOIC	R-20

CAUTION

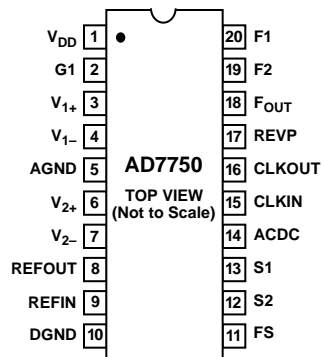
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7750 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Descriptions
1	V _{DD}	Power Supply Pin, 5 V nominal \pm 5% for specifications.
2	G1	Gain Select, Digital Input. This input selects the gain for the Channel 1 differential input. When G1 is low, the gain is 1 and when G1 is high, the gain is 16. See Analog Inputs section.
3, 4	V ₁₍₊₎ , V ₁₍₋₎	Channel 1 Differential Inputs. See the Analog Inputs section for an explanation of the maximum input signal ranges. Channel 1 has selectable gains of 1 and 16. The absolute maximum rating is \pm 6 V for each pin. The recommended clamp voltage for external protection circuitry is \pm 5 V.
5	AGND	The Analog Ground reference level for Channels 1 and 2 differential input voltages. Absolute voltage range relative to DGND pin is -20 mV to $+20$ mV. The Analog Ground of the PCB should be connected to digital ground by connecting the AGND pin and DGND pin together at the DGND pin.
6, 7	V ₂₍₊₎ , V ₂₍₋₎	Channel 2 Differential Inputs. See the Analog Inputs section for an explanation of the maximum input signal ranges. Channel 2 has a fixed gain of 2. The absolute maximum rating is \pm 6 V for each pin. The recommended clamp voltage for external protection circuitry is \pm 5 V.
8	REFOUT	Internal Reference Output. The AD7750 can use either its own internal 2.5 V reference or an external reference. For operation with the internal reference this pin should be connected to the REFIN pin.
9	REFIN	Reference Input. The AD7750 can use either its own internal 2.5 V reference or an external reference. For operation with an external reference, a 2.5 V \pm 8%, reference should be applied at this pin. For operation with an internal reference, the REFOUT pin should be connected to this input. For both internal or external reference connections, an input filtering capacitor should be connected between the REFIN pin and Analog Ground.
10	DGND	The Ground and Substrate Supply Pin, 0 V. This is the reference ground for the digital inputs and outputs. These pins should have their own ground return on the PCB, which is joined to the Analog Ground reference at one point, i.e., the DGND pin.
11	FS	Frequency Select, Digital Input. This input, along with S1 and S2, selects the operating mode of the AD7750—see Table I.
13, 12	S1, S2	Mode Selection, Digital Inputs. These pins, along with FS, select the operating mode of the AD7750—see Table I.
14	ACDC	High-Pass Filter Control Digital Input. When this pin is high, the high-pass filter is switched into the signal path of Channel 1. When this pin is low, the high-pass filter is removed. Note when the filter is off there is a fixed time delay between channels; this is explained in the Functional Description section.
15	CLKIN	An external clock can be provided at this pin. Alternatively, a crystal can be connected across CLKIN and CLKOUT for the clock source. The clock frequency is 3.58 MHz for specified operation.
16	CLKOUT	When using a crystal, it must be connected across CLKIN and CLKOUT. The CLKOUT can drive only one CMOS load when CLKIN is driven externally.
17	REVP	Reverse Polarity, Digital Output. This output becomes active high when the polarity of the signal on Channel 1 is reversed. This output is reset to zero at power-up. This output becomes active only when there is a pulse output on F1 or F2. See Reverse Polarity Indicator section.
18	F _{OUT}	High-Speed Frequency Output. This is also a fixed-width pulse stream that is synchronized to the AD7750 CLKIN. The frequency is proportional to the product of Channel 1 and Channel 2 or the signal on either channel, depending on the operating mode—see Table I. The output format is an active high pulse approximately 90 ms wide—see Digital-to-Frequency Conversion section.
20, 19	F1, F2	Frequency Outputs. F1 and F2 provide fixed-width pulse streams that are synchronized to the AD7750 CLKIN. The frequency is proportional to the product of Channel 1 and Channel 2—see Table I. The output format is an active low pulse approximately 275 ms wide—see Digital-to-Frequency Conversion section.

**PIN CONFIGURATION
SOIC and DIP**



Typical Performance Characteristics

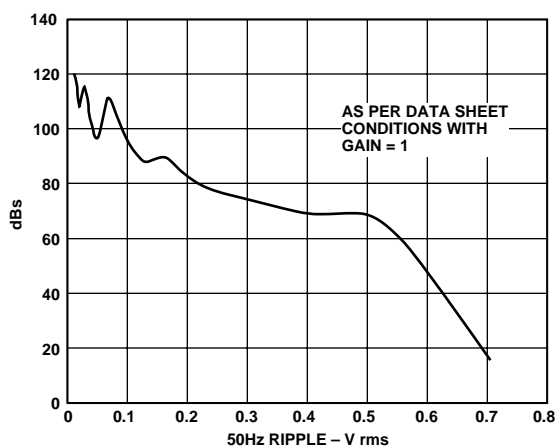


Figure 1. PSR as a Function of V_{DD} 50 Hz Ripple

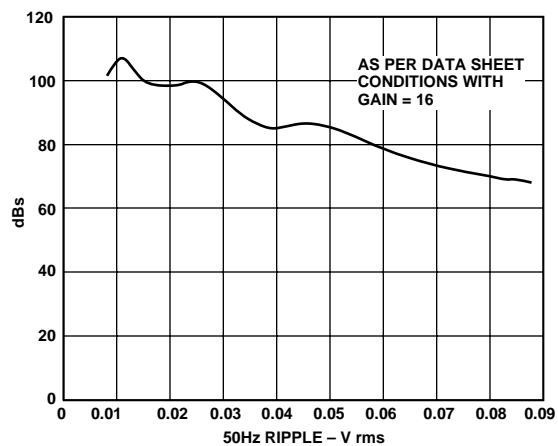


Figure 3. PSR as a Function of V_{DD} 50 Hz Ripple

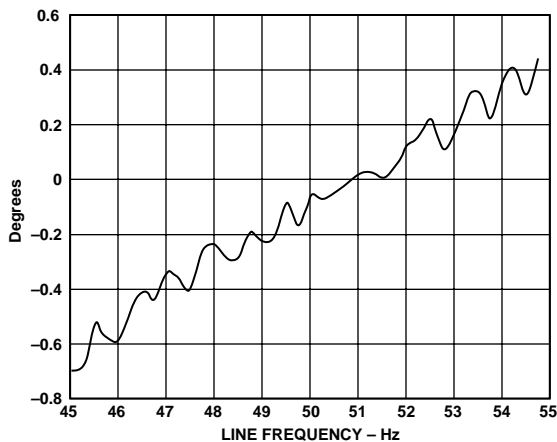


Figure 2. Phase Error as a Function of Line Frequency

AD7750

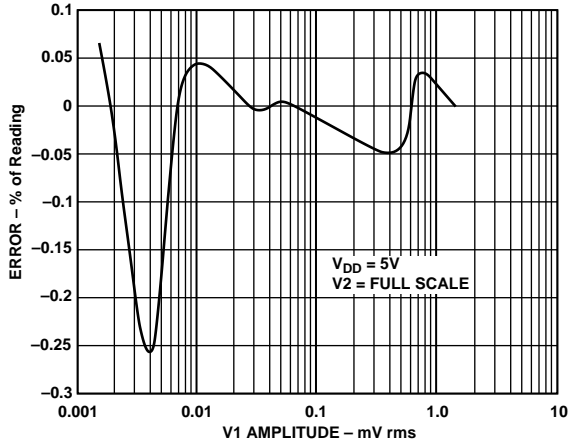


Figure 4. Error as a Percentage (%) of Reading Over a Dynamic Range of 1000, Gain = 1

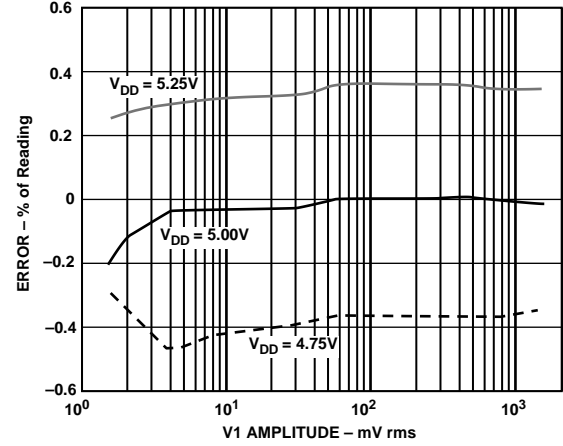


Figure 6. Measurement Error vs. Input Signal Level and Varying V_{DD} with Channel 1, Gain = 1

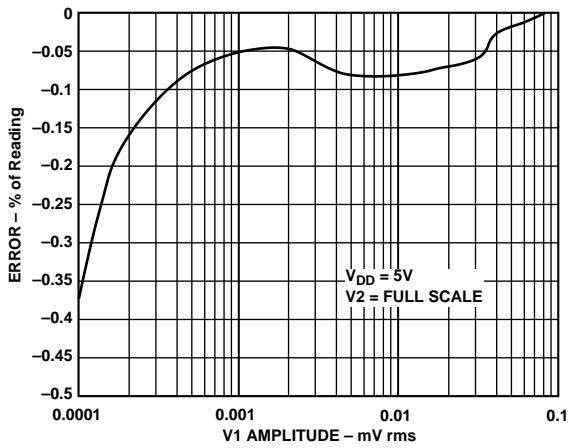


Figure 5. Error as a Percentage (%) of Reading Over a Dynamic Range of 1000, Gain = 16

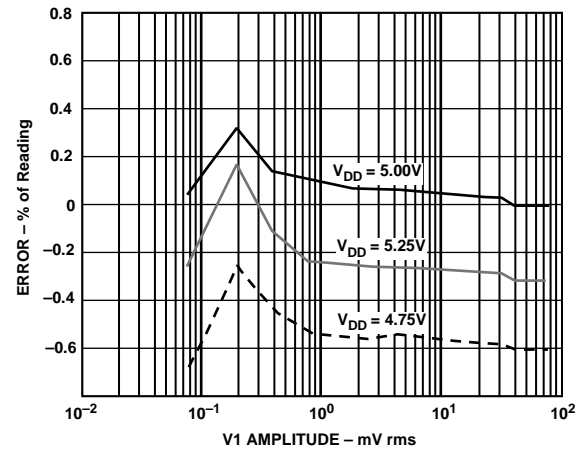


Figure 7. Measurement Error vs. Input Signal Level and Varying V_{DD} with Channel 1, Gain = 16

ANALOG INPUTS

The analog inputs of the AD7750 are high impedance bipolar voltage inputs. The four voltage inputs make up two truly differential voltage input channels called V_1 and V_2 . As with any ADC, an antialiasing filter or low-pass filter is required on the analog input. The AD7750 is designed with a unique switched capacitor architecture that allows a bipolar analog input with a single 5 V power supply. The four analog inputs (V_{1+} , V_{1-} , V_{2+} , V_{2-}) each have a voltage range from -1.0 V to $+1.0$ V. This is an absolute voltage range and is relative to the ground (AGND) pin. This ground is nominally at a potential of 0 V relative to the board level ground. Figure 8 shows a very simplified diagram of the analog input structure. When the analog input voltage is sampled, the switch is closed and a very small sampling capacitor is charged up to the input voltage. The resistor in the diagram can be thought of as a lumped component made up of the on resistance of various switches.

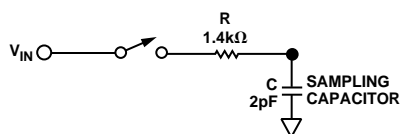


Figure 8. Equivalent Analog Input Circuit

Analog Inputs Protection Circuitry

The analog input section also has protection circuitry. Since the power supply rails are 0 V to 5 V, the analog inputs can no longer be clamped to the supply rails by diodes. Thus, the internal protection circuitry monitors the current paths during a fault condition and protects the device from continuous overvoltage, continuous undervoltage and ESD events. The maximum overvoltage the AD7750 analog inputs can withstand without causing irreversible damage is ± 6 V relative to AGND pin.

In the case of continuous overvoltage and undervoltage the series resistance of the antialiasing filter can be used to limit input current. The total input current in the case of a fault should be limited to 10 mA.

For normal operation of the AD7750 there are two further restrictions on the signal levels presented to the analog inputs.

1. The voltage on any input relative to the AGND pin must not exceed ± 1 V.
2. The differential voltage presented to the ADC (Analog Modulator) must not exceed ± 2 V.

In Figure 12, Channel 1 has a peak voltage on V_{1+} and V_{1-} of ± 1 V. These signals are not gained ($G1 = 0$) and so the differential signal presented to the modulator is ± 2 V. However, Channel 2 has an associated gain of two and so care must be taken to ensure the modulator input does not exceed ± 2 V. Therefore, the maximum signal voltage that can appear on V_{2+} and V_{2-} is ± 0.5 V.

The difference between single-ended and complementary differential input schemes is shown in the diagram below, Figure 9. For a single-ended input scheme the V_- input is held at the same potential as the AGND Pin. The maximum voltages can then be applied to the V_+ input are shown in Figures 10 and 11. An example of this input scheme uses a shunt resistor to convert the line current to a voltage that is then applied to the V_{1+} input of the AD7750.

An example of the complementary differential input scheme uses a current transformer to convert the line current to a voltage that is then applied to V_{1+} and V_{1-} . With this scheme the voltage on the V_+ input is always equal to, but of opposite polarity to the voltage on V_- . The maximum voltage that can be applied to the inputs of the AD7750 using this scheme is shown in Figures 12 and 13.

Note that the common mode of the analog inputs must be driven. The output terminals of the CT are, therefore, referenced to ground.

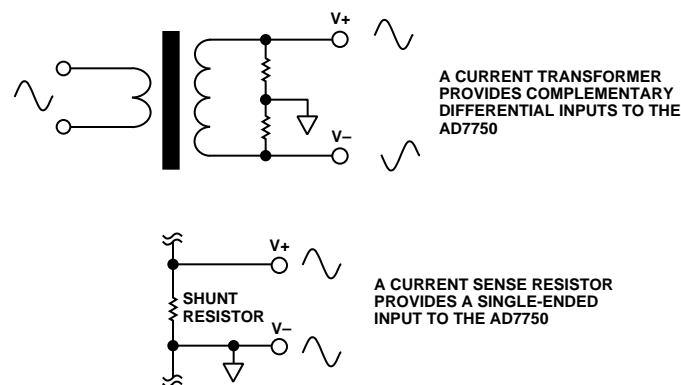


Figure 9. Examples of Complementary and Single-Ended Input Schemes

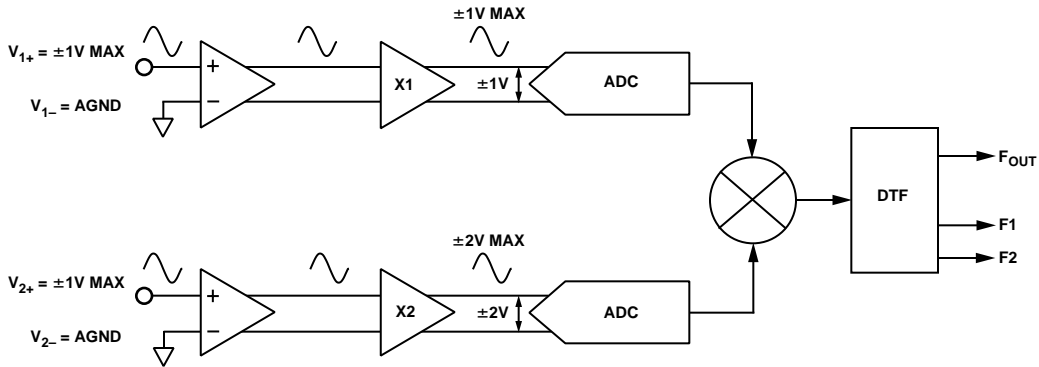


Figure 10. Maximum Input Signals with Respect to AGND for a Single-Ended Input Scheme, $G1 = 0$

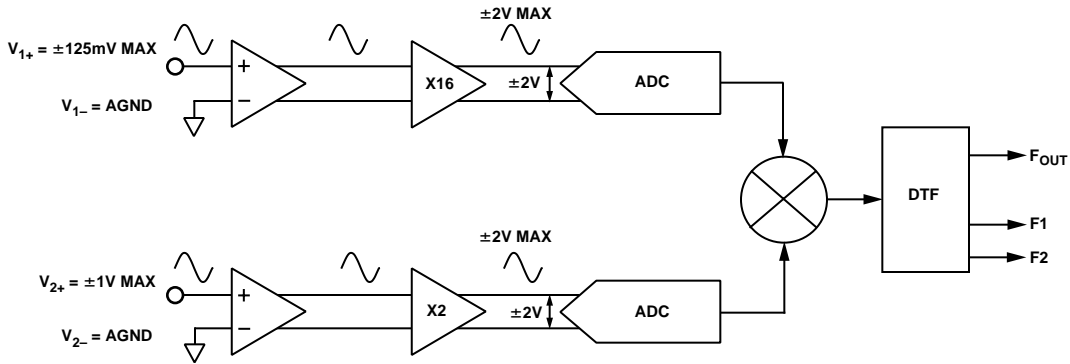


Figure 11. Maximum Input Signals with Respect to AGND for a Single-Ended Input Scheme, $G1 = 1$

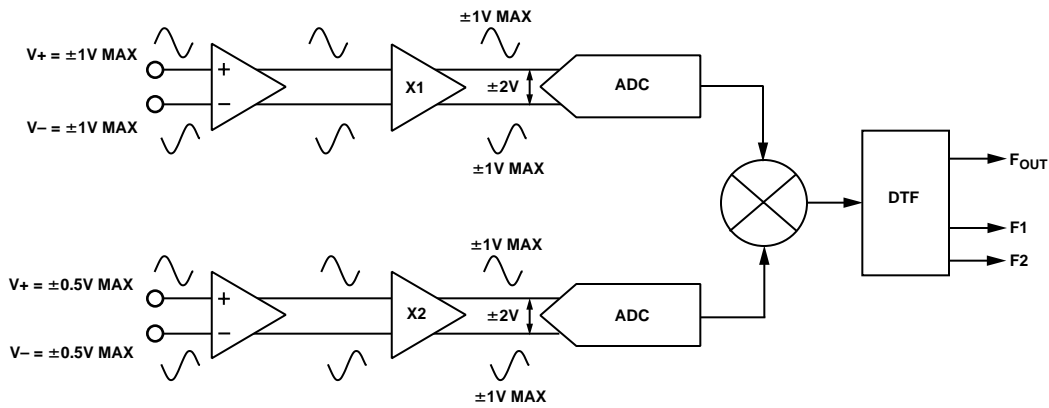


Figure 12. Maximum Input Signals for a Complementary Input Scheme, $G1 = 0$

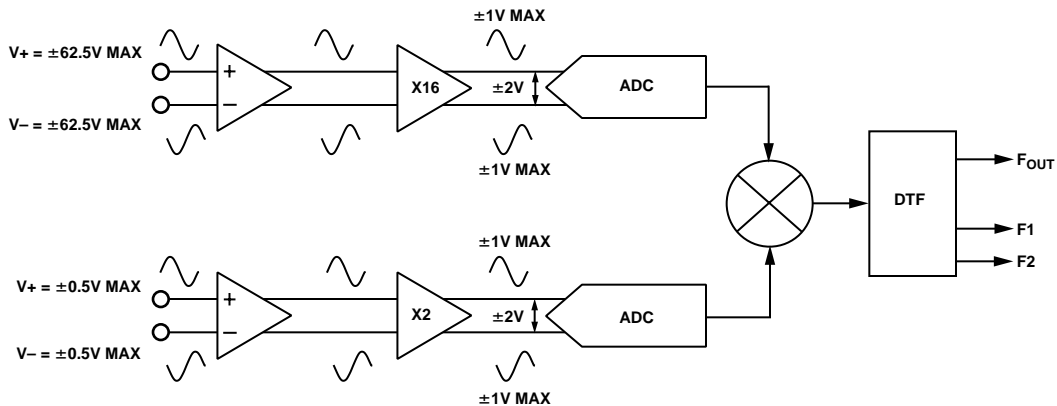


Figure 13. Maximum Input Signals for a Complementary Input Scheme, $G1 = 1$

DETERMINING THE OUTPUT FREQUENCIES OF THE AD7750

F_{OUT} , F_1 and F_2 are the frequency outputs of the AD7750. The output frequencies of the AD7750 are a multiple of a binary fraction of the master clock frequency $CLKIN$. This binary fraction of the master clock is referred to as F_{MAX} in this data

sheet. F_{MAX} can have one of two values, F_{MAX1} and F_{MAX2} , depending on which mode of operation the AD7750 is in. The operating modes of the AD7750 are selected by the logic inputs FS , S_2 and S_1 . The table below outlines the F_{MAX} frequencies and the transfer functions for the various operating modes of the AD7750.

Table I. Operating Mode

Mode	FS	S2	S1	Mode Description	F1, F2 ¹ (Hz)	F _{OUT} ¹ (Hz)	F _{MAX}
0	0	0	0	Power Measurement Mode. Four Quadrant Multiplication (Sign and Magnitude Output).	$F_{MAX1} \pm k.F_{MAX1}$	16. $[F_{MAX1} \pm k.F_{MAX1}]$	$F_{MAX1} = CLKIN/2^{19}$ $F_{MAX1} = 6.8 \text{ Hz}$
1	0	0	1	Power Measurement Mode. Two Quadrant Multiplication (Magnitude Only).	0 to $k.F_{MAX1}$	8. $[0 \text{ to } k.F_{MAX1}]$	$F_{MAX1} = CLKIN/2^{19}$ $F_{MAX1} = 6.8 \text{ Hz}$
2	0	1	0	Power Measurement Mode. Two Quadrant Multiplication (Magnitude Only).	0 to $k.F_{MAX1}$	16. $[0 \text{ to } k.F_{MAX1}]$	$F_{MAX1} = CLKIN/2^{19}$ $F_{MAX1} = 6.8 \text{ Hz}$
3 ²	0	1	1	V ₁ Channel Monitor Mode on F _{OUT} . Power Measurement Mode on F1, F2 (Sign and Magnitude Output).	$F_{MAX1} \pm k.F_{MAX1}$	32. $[F_{MAX1} \pm k^2.F_{MAX1}]$	$F_{MAX1} = CLKIN/2^{19}$ $F_{MAX1} = 6.8 \text{ Hz}$
4	1	0	0	Power Measurement Mode. Four Quadrant Multiplication (Sign and Magnitude Output).	$F_{MAX2} \pm k.F_{MAX2}$	16. $[F_{MAX2} \pm k.F_{MAX2}]$	$F_{MAX2} = CLKIN/2^{18}$ $F_{MAX2} = 13.6 \text{ Hz}$
5	1	0	1	Power Measurement Mode. Two Quadrant Multiplication (Magnitude Only).	0 to $k.F_{MAX2}$	16. $[0 \text{ to } k.F_{MAX2}]$	$F_{MAX2} = CLKIN/2^{18}$ $F_{MAX2} = 13.6 \text{ Hz}$
6	1	1	0	Power Measurement Mode. Two Quadrant Multiplication (Magnitude Only).	0 to $k.F_{MAX2}$	32. $[0 \text{ to } k.F_{MAX2}]$	$F_{MAX2} = CLKIN/2^{18}$ $F_{MAX2} = 13.6 \text{ Hz}$
7 ²	1	1	1	V ₂ Channel Monitor Mode on F _{OUT} . Power Measurement Mode on F1, F2 (Sign and Magnitude Output).	$F_{MAX2} \pm k.F_{MAX2}$	16. $[F_{MAX2} \pm k^2.F_{MAX2}]$	$F_{MAX2} = CLKIN/2^{18}$ $F_{MAX2} = 13.6 \text{ Hz}$

NOTES

¹The variable k is proportional to the product of the rms differential input voltages on Channel 1 and Channel 2 (V_1 and V_2).

$$k = (1.32 \times V_1 \times V_2 \times \text{Gain}) / V_{REF}^2$$

²Applies to F_{OUT} only. The variable k is proportional to the instantaneous differential input voltage on Channel 1 ($FS = 0, S_1 = 1, S_0 = 1$) or the instantaneous differential voltage on Channel 2 ($FS = 1, S_1 = 1, S_0 = 1$), i.e., Channel Monitor Mode.

$$k = (0.81 \times V) / V_{REF}$$

$$V = V_1 \times \text{Gain} \text{ or}$$

$$V = V_2 \times 2$$

NOTE: V_1 and V_2 here refer to the instantaneous differential voltage on Channel 1 or Channel 2, not the rms value.

Mode Description (Table I)

The section of Table I labeled Mode Description summarizes the functional modes of the AD7750. The AD7750 has two basic modes of operation, i.e., four and two quadrant multiplication. The diagram in Figure 14 is a graphical representation of the transfer functions for two and four quadrant multiplication.

Four Quadrant Multiplication (Modes 0, 3, 4 and 7)

When the AD7750 is operating in its four quadrant multiplication mode the output pulse frequency on F_1 , F_2 and F_{OUT} contains both sign and magnitude information. The magnitude information is indicated by the output frequency variation ($k.F_{MAX}$) from a center frequency (F_{MAX}). The sign information is indicated by the sign of the frequency variation around F_{MAX} . For example if the output frequency is equal to $F_{MAX} - k.F_{MAX}$ then the magnitude of the product is given by $k.F_{MAX}$ and it has a negative sign.

Two Quadrant Multiplication (Modes 1, 2, 5 and 6)

When operating in this mode the output pulse frequency only contains magnitude information. Again as in the case of four

quadrant multiplication the magnitude information is included in the output frequency variation ($k.F_{MAX}$). However, in this mode the zero power frequency is 0 Hz, so the output frequency variation is from 0 Hz to ($k.F_{MAX}$) Hz. Also note that a no-load threshold and the reverse polarity indicator are implemented in these modes see No Load Threshold and Reverse Polarity Indicator sections. These modes are the most suitable for a Class 1 meter implementation.

Channel Monitor Modes (Modes 3 and 7)

In this mode of operation the F_{OUT} pulse frequency does not give product information. When $FS = 0$, the F_{OUT} output frequency gives sign and magnitude information about the voltage on Channel 1. When $FS = 1$ the F_{OUT} output frequency gives sign and magnitude information about the voltage on Channel 2.

Note the F_1 , F_2 pulse outputs still continue to give power information.

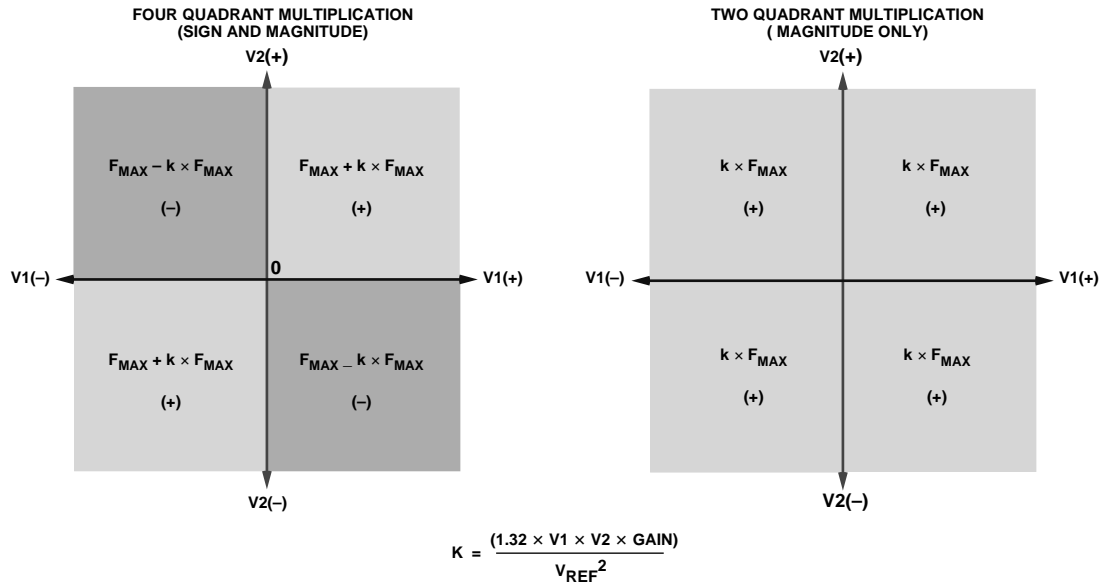


Figure 14. Transfer Functions (Four and Two Quadrant Multiplication)

Maximum Output Frequencies

Table II shows the maximum output frequencies of F_{OUT} and F_1 , F_2 for the various operating modes of the AD7750. The table shows the maximum output frequencies for dc and ac input signals on V_1 and V_2 . When an ac signal (sinusoidal) is applied to V_1 and V_2 the AD7750 produces an output frequency which is proportional to the product of the rms value of these inputs. If two ac signals with peak differential values of $V_{1\text{MAX}}$ and $V_{2\text{MAX}}$ are applied to Channels 1 and 2, respectively, then the output frequency is proportional to $V_{1\text{MAX}}/\sqrt{2} \times V_{2\text{MAX}}/\sqrt{2} = (V_{1\text{MAX}} \times V_{2\text{MAX}})/2$. If $V_{1\text{MAX}}$ and $V_{2\text{MAX}}$ are also the maximum dc input voltages then the maximum output frequencies for ac signals will always be half that of dc input signals. Example calculation of F_1 , F_2 max for Mode 2 and Gain = 1. The maximum input voltage (dc) on Channel 1 is 2 V ($V_{1+} = +1$ V, $V_{1-} = -1$ V)—see Analog Inputs section. The maximum input voltage on Channel 2 is 1 V. Using the transfer function:

$$k = (1.32 \times V_1 \times V_2 \times \text{Gain}) / V_{\text{REF}}^2$$

$$k = 0.4224$$

$$F_1, F_2 = k \cdot 6.8 \text{ Hz} = 2.9 \text{ Hz}$$

FUNCTIONAL DESCRIPTION

The AD7750 combines two analog-to-digital converters, a digital multiplier, digital filters and a digital-to-frequency (DTF) converter onto one low cost integrated circuit. The AD7750 is fabricated on a double poly CMOS process (0.6 μ) and retains its high accuracy by performing all multiplications and manipulations in the digital domain. The schematic in Figure 15 shows an equivalent circuit for the AD7750 signal processing chain. The first thing to notice is that the analog signals are first converted to digital signals by the two second-order sigma-delta modulators. All subsequent signal processing is carried out in the digital domain. The main source of errors in an application is therefore in the analog-to-digital conversion process. For this

reason great care must be taken when interfacing the analog inputs of the AD7750 to the transducer. This is discussed in the Applications section.

HPF in Channel 1

To remove any dc offset that may be present at the output modulator 1, a user selectable high-pass IIR filter (Pin ACDC) can be introduced into the signal path. This HPF is necessary when carrying out power measurements. However, this HPF has an associated phase lead given by $90^\circ - \tan^{-1}(f/2.25)$. Figure 16 shows the transfer function of the HPF in Channel 1. The Phase lead is 2.58° at 50 Hz. In order to equalize the phase difference between the two channels a fixed time delay is introduced. The time delay is set at 143 μ s, which is equivalent to a phase lag of -2.58° at 50 Hz. Thus the cumulative phase shift through Channel 1 is 0° .

Because the time delay is fixed, external phase compensation circuitry will be required if the line frequency differs from 50 Hz. For example with a line frequency of 60 Hz the phase lead due to the HPF is 2.148° and the phase lag due to the fixed time delay is 3.1° . This means there is a net phase lag in Channel 1 of 0.952° . This phase lag in Channel 1 can be compensated for by using a phase lag compensation circuit like the one shown in Figure 17. The phase lag compensation is placed on Channel 2 (voltage channel) to equalize the channels. The antialiasing filter associated with Channel 1 (see Applications section) produces a phase lag of 0.6° at 50 Hz; therefore, to equalize the channels, a net phase lag of $(0.6^\circ + 0.952^\circ) 1.552^\circ$ should be in place on Channel 2. The gain trim resistor VR1 (100 Ω) produces a phase lag variation of 1.4° to 1.5° with VR2 = 0 Ω . VR2 can add an additional 0.1° phase lag (VR2 = 200 Ω).

Table II. Maximum Output Frequencies

Mode	FS	S2	S1	F1, F2 (Hz) (DC)	F _{OUT} (Hz) (DC)	F1, F2 (Hz) (AC)	F _{OUT} (Hz) (AC)
0	0	0	0	6.8 ± 2.9	109 ± 46	6.8 ± 1.45	109 ± 23
1	0	0	1	0 to 2.9	0 to 23	0 to 1.45	0 to 11.5
2	0	1	0	0 to 2.9	0 to 46	0 to 1.45	0 to 23
3	0	1	1	6.8 ± 2.9	218 ± 142	6.8 ± 1.45	218 ± 142
4	1	0	0	13.6 ± 5.8	218 ± 92	13.6 ± 2.9	218 ± 46
5	1	0	1	0 to 5.8	0 to 92	0 to 2.9	0 to 46
6	1	1	0	0 to 5.8	0 to 184	0 to 2.9	0 to 92
7	1	1	1	13.6 ± 5.8	218 ± 142	13.6 ± 2.9	218 ± 142

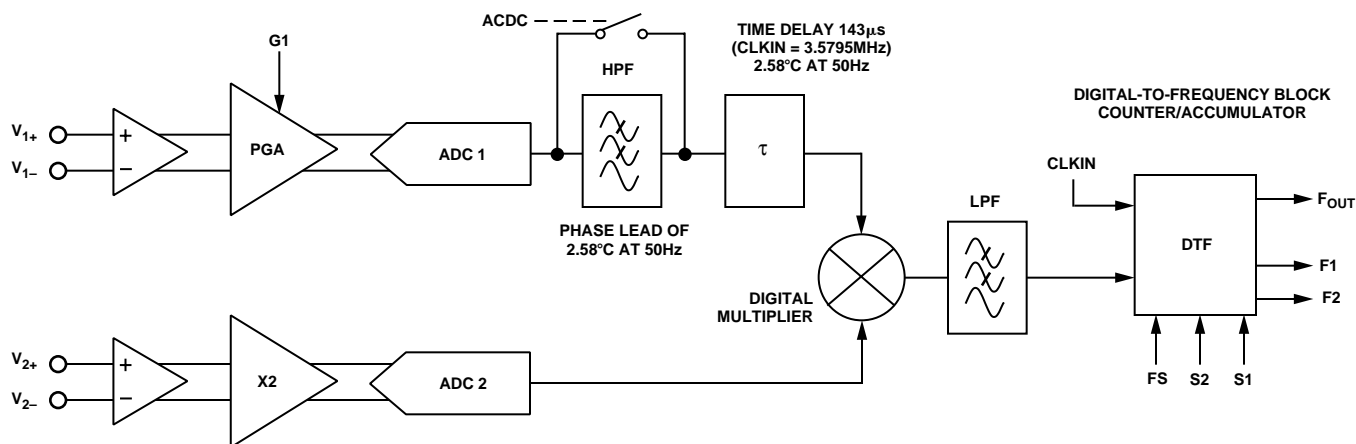


Figure 15. Equivalent AD7750 Signal Processing Chain

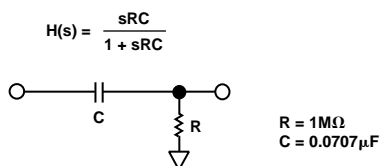


Figure 16. HPF in Channel 1

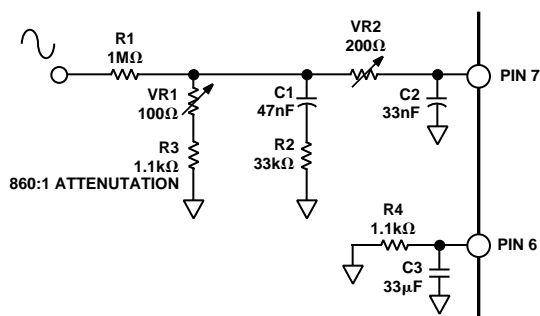


Figure 17. Phase Lag Compensation on Channel 1 for 60 Hz Line Frequency

Digital-to-Frequency Converter (DTF)

After they have been filtered, the outputs of the two sigma-delta modulators are fed into a digital multiplier. The output of the multiplier is then low-pass filtered to obtain the real power information. The output of the LPF enters a digital-to-frequency converter whose output frequency is now proportional to the real power. The DTF offers a range of output frequencies to suit most power measurement applications. There is also a high frequency output called F_{OUT}, which can be used for calibration purposes. The output frequencies are determined by the logic inputs FS, S2 and S1. This is explained in the section of this data sheet called Determining the Output Frequencies of the AD7750.

Figure 18 shows the waveforms of the various frequency outputs. The outputs F1 and F2 are the low frequency outputs that can be used to directly drive a stepper motor or electromechanical pulse counter. The F1 and F2 outputs provide two alternating low going pulses. The pulsewidth is set at 275 ms and the time between the falling edges of F1 and F2 is approximately half the period of F1. If, however, the period of F1 and F2 falls below 550 ms (1.81 Hz) the pulsewidth of F1 and F2 is set to half the period. For example in Mode 3, where F1 and F2 vary around 6.8 Hz, the pulsewidth would vary from 1/2.(6.8+1.45) seconds to 1/2.(6.8-1.45) seconds—see Table II.

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The high frequency F_{OUT} output is intended to be used for communications (via IR LED) and calibration purposes. F_{OUT} produces a 90 ms wide pulse at a frequency that is proportional to the product of Channel 1 and Channel 2 or the instantaneous voltage on Channel 1 or Channel 2. The output frequencies are given in Table I in the Determining the Output Frequencies of the AD7750 section of this data sheet. As in the case of F1 and F2, if the period of F_{OUT} falls below 180 ms, the F_{OUT} pulsewidth is set to half the period. For example, if the F_{OUT} frequency is 20 Hz, the F_{OUT} pulsewidth is 25 ms.

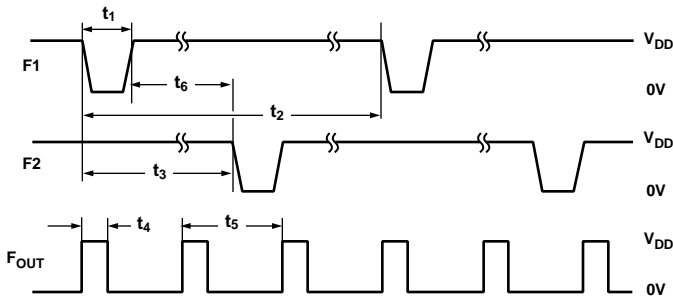


Figure 18. Timing Diagram for Frequency Outputs

VOLTAGE REFERENCE

The AD7750 has an on-chip temperature compensated band-gap voltage reference of 2.5 V with a tolerance of ± 250 mV. The temperature drift for the reference is specified at 50 ppm/ $^{\circ}$ C. It should be noted that this reference variation will cause a frequency output variation from device to device for a given set of input signals. This should not be a problem in most applications since it is a straight gain error that can easily be removed at the calibration stage.

REVERSE POLARITY INDICATOR

When the AD7750 is operated in a Magnitude Only mode of operation (i.e., Modes 1, 2, 5 and 6), and the polarity of the power changes, the logic output REVP will go high. However, the REVP pin is only activated when there is pulse output on F1 or F2. Therefore, if the power being measured is low, it may be some time before the REVP pin goes logic high even though the polarity of the power is reversed. Once activated the REVP output will remain high until the AD7750 is powered down.

APPLICATIONS INFORMATION

Designing a Single Phase Class 1 Energy Meter (IEC 1036)

The AD7750 Product-to-Frequency Converter is designed for use in a wide range of power metering applications. In a typical power meter two parameters are measured (i.e., line voltage and current) and their product obtained. The real power is then obtained by low-pass filtering this product result. The line voltage can be measured through a resistor divider or voltage transformer, and the current can be sensed and converted to a voltage through a shunt resistor, current transformer or hall effect device.

The design methodology used in the following example is to use the upper end of the current channel dynamic range, i.e., Channel 1 of the AD7750. The assumption here is that the signal on the voltage channel will remain relatively constant while the signal on the current channel will vary with load. Using the upper end of the dynamic range of Channel 1 will improve the

meter accuracy with small load currents. Hence an error of less than 1% from 4% I_b to 400% I_b will be easier to achieve.

We will assume the design of a Class 1 meter. The specification (IEC1036) requires that the meter have an error of no greater than 1% over the range 4% I_b to 400% I_b (I_{MAX}), where I_b is the basic current¹. In addition, we will design a meter that accommodates signals with a crest factor of 2. The crest factor is the ratio of V_{PEAK}/V_{rms} . A pure sinusoidal waveform has a crest of $\sqrt{2} = 1.414$ and an undistorted triangular waveform has a crest factor of $\sqrt{3} = 1.73$. Using a gain of 1 on Channel 1 the maximum differential signal which can be applied to Channel 1 is ± 2 V—See Analog Input Ranges section. With a crest factor of 2 the maximum rms signal on Channel 1 is, therefore, 1 V rms (equivalent to I_{MAX}). The smallest signal (4% I_b) appearing on Channel 1 is therefore 10 mV rms.

Load Current	Channel 1
4% I_b	10 mV rms
I_b	250 mV rms
400% I_b	1 V rms

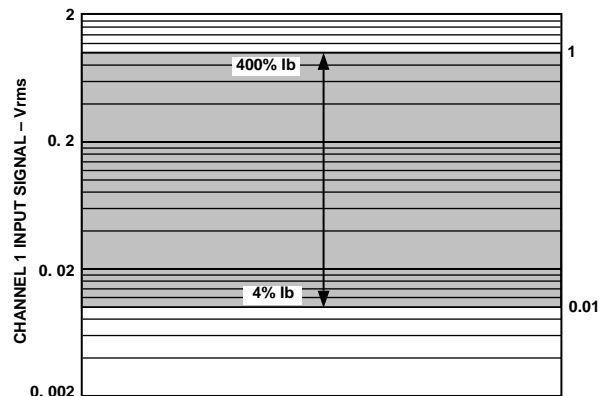


Figure 19. Use the Upper End of the Dynamic Range of Channel 1 (Current)

Calculations for a 100 PPKWHR Meter

The AD7750 offers a range of maximum output frequencies—see Table I and Table II. In the Magnitude Only modes of operation the two maximum output frequencies are 1.45 Hz and 2.9 Hz. The signal on the voltage channel (Channel 2) is scaled to achieve the correct output pulse frequency for a given load (e.g., 100 PPKWHR). The relationship between the input signals and the output frequency is given by the equation:

$$Freq = k \times F_{MAX}$$

$$where k = (1.32 \times V_1 \times V_2 \times Gain) / V_{REF}^2$$

F_{MAX} = 6.8 Hz or 13.6 Hz depending on the mode—see Table I, $Gain$ is the gain of Channel 1, V_1 and V_2 are the differential voltages on Channels 1 and 2 and V_{REF} is the reference voltage (2.5 V \pm 8%).

To design a 100 PPKWHR meter with $I_b = 15$ A rms and a line voltage of 220 V rms the output pulse frequency with a load current of I_b is 0.0916 Hz (See Calculation 1 below).

Therefore, 0.0916 Hz = $k \times 6.8$ Hz (Mode 2) or $k = 0.01347$.

With a load current of I_b the signal on Channel 1 (V_1) is equal to 0.25 V rms (remember 400% $I_b = 1$ V rms) and, therefore, the signal on Channel 2 (V_2) is equal to 0.255 V rms (See Calculation 2). This means that the nominal line voltage (220 V rms) needs to be attenuated by approximately 860, i.e., $220/0.255$.

¹See IEC 1036 2nd Edition 1996-09 Section 3.5.1.1.

For 100 PPKWHR V_2 is equal to 0.255 V rms or the line voltage attenuated by a factor of 860.

Calculation 1

$$100 \text{ PPKWHR} = 0.02777 \text{ Hz/kW.}$$

lb of 15 A rms and line voltage of 220 V = 3.3 kΩ. Hence, the output frequency is given by $3.3 \times 0.02777 \text{ Hz} = 0.0916 \text{ Hz}$.

Calculation 2

$$k = (1.32 \times V_1 \times V_2 \times \text{Gain}) / V_{\text{REF}}^2.$$

$$0.01347 = (1.32 \times 0.25 \times V_2 \times 1) / 6.25.$$

$$V_2 = 0.255.$$

Figure 21 below shows how the design equations from the previous page are implemented.

Measuring the Load Current

The load current is converted to a voltage signal for Channel 1 using a CT (Current Transformer). A 15 A rms load should produce a 250 mV rms signal on Channel 1. A CT with a turns ratio of 120 and a shunt resistor of 2 Ω. will carry out the necessary current to voltage conversion. The CT and its shunt resistance should be placed as close as possible to the AD7750. This will improve the accuracy of the meter at very small load currents. At small load currents the voltage levels on Channel 1 are in the order of 10 mV and the meter is more prone to error due to stray signal “pick up.” When measuring power the HPF in the current channel must be switched on. This is done by connecting the ACDC pin to V_{DD} .

NOTE: The voltage signals on V_{1+} and V_{1-} must be referenced to ground. This can be achieved as shown in Figure 21 below, i.e., by referencing $1/2 R_{\text{CT}}$ to ground or by connecting a centertap on the CT secondary to ground.

Measuring the Line Voltage

When the AD7750 is biased around the live wire as shown in Figure 21, the task of measuring the line voltage is greatly simplified. A resistor divider attenuates the line voltage and provides a single-ended input for Channel 2. The component values of the divider are chosen to give the correct rating (e.g., 100 PPKWHR) for the meter. See the design equations on the previous page. For this design an attenuation ratio of 860:1 is required.

Antialiasing Components Channels 1 and 2

The AD7750 is basically two ADCs and a digital multiplier. As with any ADC, a LPF (Low-Pass Filter) should be used on the analog inputs to avoid out of band signal being aliased into the band of interest. In the case of a Class 1 meter the band of interest lies in the range 48 Hz to 1 kHz approximately. The components R3, R4, R6, R7, C5, C6, C9 and C10 make up the LPFs on each of the four analog inputs. Note that although Channel 2 is used single ended a LPF is still required on V_{2-} .

Power Supply Circuit

The AD7750 operates from a single power supply of $5 \text{ V} \pm 5\%$ but still accommodates input signals in the range $\pm 1 \text{ V}$. Because the AD7750 doesn't require dual supplies the number of external components for the power supply is reduced. One of the most important design goals for the power supply is to ensure that the ripple on the output is as low as possible. Every analog or mixed signal IC is to a greater or lesser extent susceptible to power supply variations. Power supply variations or ripple, if large enough, may affect the accuracy of the device when measuring small signals. The plot in Figure 20 shows the ripple associated with the circuit in Figure 21. The ripple is in the region of 10 mV peak to peak.

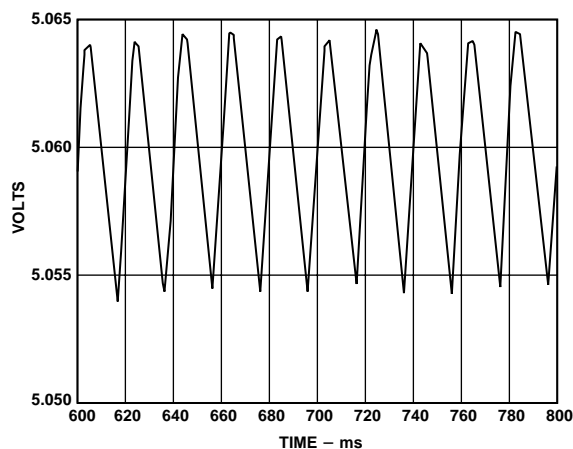


Figure 20. Power Supply Ripple

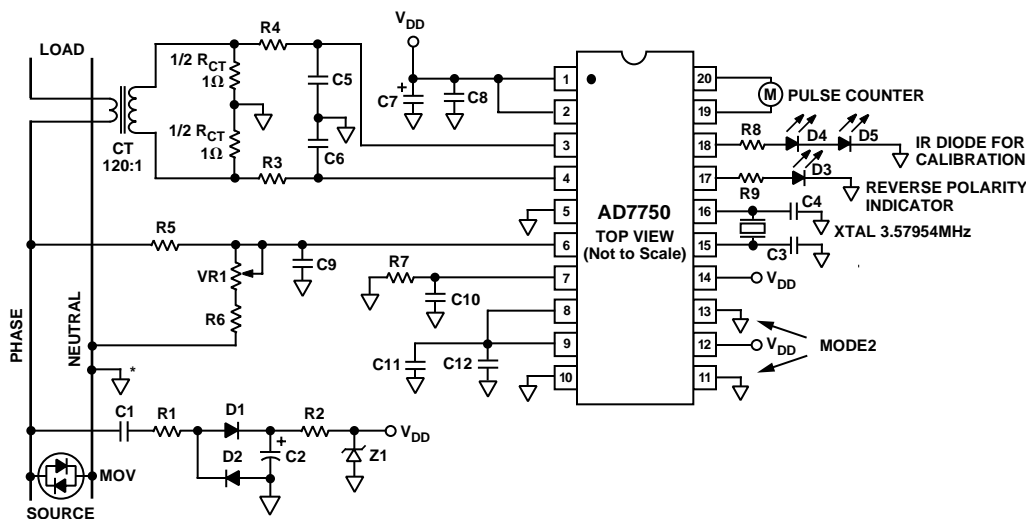


Figure 21. Suggested Class 1 Meter Implementation

AD7750

Registering the Power Output

The low frequency pulse outputs (F1 and F2) of the AD7750 provide the frequency output from the product-to-frequency conversion. These outputs can be used to drive a stepper motor or impulse counter.

A high frequency output is available at the pin F_{OUT} . This high frequency output is used for calibration purposes. In Mode 2 the output frequency is $16 \times F1(2)$. With a load current of I_b the frequency at F_{OUT} will be 1.4656 Hz ($0.0916 \text{ Hz} \times 16$ from calculations). If a higher frequency output is required, the FS pin can be set to V_{DD} 5 V for calibration. In this case the output frequency is equal to $64 \times F1$ or 5.8624 Hz at I_b —see Table I.

NO LOAD THRESHOLD OF THE AD7750

The AD7750 will detect when the power drops below a certain level. When the power (current) drops below a predefined threshold the AD7750 will cease to generate an output drive for the stepper motor (F1, F2). This feature of the AD7750 is intended to reproduce the behavior of Ferraris meters. A Ferraris meter will have friction associated with the wheel rotation, therefore the wheel will not rotate below a certain power level. The no load threshold is only implemented in the Magnitude Only modes (Modes 1, 2, 5 and 6—see Table I). The IEC1036 specification includes a test for this effect by requiring no output pulses during some predetermined time period. This time period is calculated as:

$$\text{time period} = 60,000/\text{pulses-per-minute}$$

If a meter is calibrated to 100 PPKWHR with a F_{OUT} running 16 times faster than F1 and F2, this time period is 37.5 minutes ($60,000/1,600$). The IEC1036 specifications state that the no load threshold must be less than the start up current level. This is specified as 0.4% of I_b .

The threshold level for a given design can be easily calculated given that the minimum output frequency of the AD7750 is 0.00048% of the maximum output frequency for a full-scale differential dc input. For example if $FS = 0$, the maximum output frequency for a full-scale dc input is 2.9 Hz (see Table II) and the minimum output frequency is, therefore, 1.39×10^{-5} Hz.

Calculating the Threshold Power (Current)

The meter used in this example is calibrated to 100 PPKWHR, has an I_b (basic current) of 15 A rms, the line voltage is 220 V rms and the turns ratio of the CT on Channel 1 is 120:1 with an 2Ω shunt resistor.

The nominal voltage on Channel 2 of the AD7750 is 255 mV rms. An F_{MAX} of 6.8 Hz is selected by setting $FS = 0$. A Magnitude Only Mode (Mode 2) is selected to enable the no load threshold. The gain on Channel 1 is set to 1. The threshold power or current can be found by using the transfer function in Table I.

$$F1, F2 = (1.32 \times V_1 \times V_2 \times \text{Gain} \times F_{MAX})/V_{REF}^2$$

From the transfer function V_1 is calculated as 37.95 μV rms—see Calculation 3.

This is equivalent to a line current of:

$$(37.95 \mu\text{V}/2 \Omega) \times 120 = 2.27 \text{ mA rms or } 0.5 \text{ W}$$

or

$$(2.27 \text{ mA}/15 \text{ A}) \times 100\% = 0.015\% \text{ of } I_b.$$

NOTE: The no load threshold as a percentage of I_b will be different for each value of I_b since the no load in watts is fixed:

$FS = 0$, the no load threshold is ($F_{MAX} = 6.8 \text{ Hz}$)
0.5 Watts for a 100 PPKWHR meter
5 Watts for a 10 PPKWHR meter

$FS = 1$, the no load threshold is ($F_{MAX} = 13.6 \text{ Hz}$)
1 Watt for a 100 PPKWHR meter
10 Watts for a 10 PPKWHR meter

Calculation 3

$$F_{MIN} = 1.32 \times V_1 \times V_2 \times \text{Gain} \times 6.8 \text{ Hz}) V_{REF}^2 \\ 1.39 \times 10^{-5} \text{ Hz} = V_1 \times 0.2555 \times 1 \times 6.8/6.25 \\ V_1 = 37.95 \mu\text{V}$$

EXTERNAL LEAD/LAG COMPENSATION

External phase compensation is often required in a power meter design to eliminate the phase errors introduced by transducers and external components. The design restriction on any external compensating network is that the network must have an overall low-pass response with a 3 dB point located somewhere between 5 kHz and 6 kHz. The corner frequency of this LPF(s) is much higher than the band of interest. The reason for this is to minimize its effect on phase variation at 50 Hz due to component tolerances.

With the antialiasing filters on all channels having the same corner (-3 dB) frequency, the main contribution to phase error will be due to the CT. A phase lead in a channel is compensated by lowering the corner frequency of the antialiasing filter to increase its associated lag and therefore cancel the lead. A phase lag in a channel should be compensated by introducing extra lag in the other channel. This can be done as previously described, i.e., moving the corner frequency of the antialiasing filters. The result in this case is that the signal on both channels has the same amount of phase lag and is therefore in phase at the analog inputs to the AD7750. The recommended RC values for the antialiasing filters on the voltage and current channels (see Antialiasing Components Channels 1 and 2) are $R = 1 \text{ k}\Omega$, $C = 33 \text{ nF}$ and $R = 100 \Omega$, $C = 330 \text{ nF}$ respectively. These values produce a phase lag of 0.6° through the filters. Varying R in the antialiasing network from 80Ω to 100Ω or 800Ω to $1 \text{ k}\Omega$ produces a phase variation from 0.475° to 0.6° at 50 Hz. This allows the user to vary the lag by 0.125° .

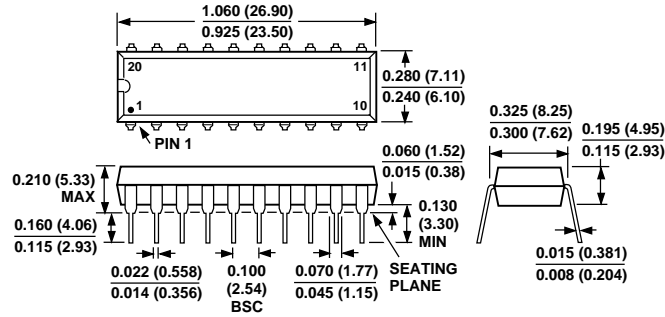
Table III. Components for Suggested Class 1 Meter Implementation in Figure 21

Schematic Designator	Description	Comments
R1	470 Ω , 5%, 1 W	These registers are required to form part of the antialiasing filtering on the analog inputs; they do not perform a voltage-to-current conversion. The choice of R5 determines the attenuation on the voltage channels and hence the meter rating, e.g., 100 PPKWHR. Forms part of the Gain Calibration network with R5 and VR1.
R2	1 k Ω , 5%, 1/2 W	
R3, R4,	100 Ω , 10%, 1/2 W	
R7	1 k Ω , 10%, 1/2 W	
R5	1 M Ω , 5%, 2 W	
R6	1.1 k Ω , 5%, 1/2 W	
R8, R9	500 Ω , 10%, 1/2 W	
VR1	100 Ω , 10/15 Turn	
C1	470 nF, 250 V ac	
C2	100 μ F, 24 V dc	
C3, C4	33 pF	Forms part of the antialiasing filters on the analog inputs.
C5, C6,	330 nF	
C9, C10	33 nF	
C7, C11	10 μ F, 10 V	
C8, C12	10 nF	
Z1	1N750	
D1, D2	1N4007	
D3	LED	
D4, D5	IR LEDS	
XTAL	3.579545 MHz	
MOV	V250PA40A	Metal Oxide Varistor–Harris Semiconductor.

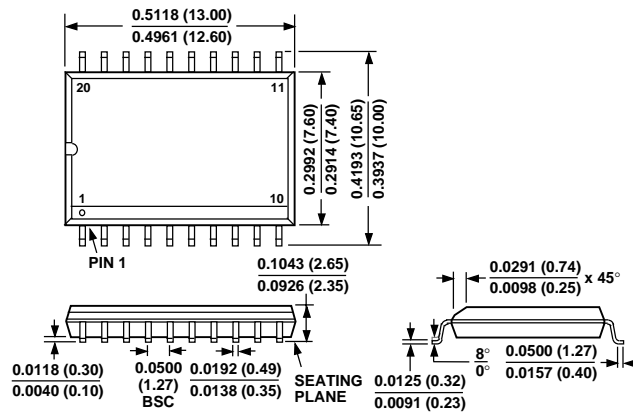
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

**20-Lead Plastic DIP
(N-20)**



**20-Lead Wide Body SOIC
(R-20)**



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