

FEATURES

Low Noise

0.9 nV/ $\sqrt{\text{Hz}}$ typ (1.2 nV/ $\sqrt{\text{Hz}}$ max) Input Voltage Noise at 1 kHz

50 nV p-p Input Voltage Noise, 0.1 Hz to 10 Hz

Low Distortion

-120 dB Total Harmonic Distortion at 20 kHz

Excellent AC Characteristics

800 ns Settling Time to 16 Bits (10 V Step)

110 MHz Gain Bandwidth (G = 1000)

8 MHz Bandwidth (G = 10)

280 kHz Full Power Bandwidth at 20 V p-p

20 V/ μs Slew Rate

Excellent DC Precision

80 μV max Input Offset Voltage

1.0 $\mu\text{V}/^\circ\text{C}$ V_{OS} Drift

Specified for ± 5 V and ± 15 V Power Supplies

High Output Drive Current of 50 mA

APPLICATIONS

Professional Audio Preamplifiers

IR, CCD, and Sonar Imaging Systems

Spectrum Analyzers

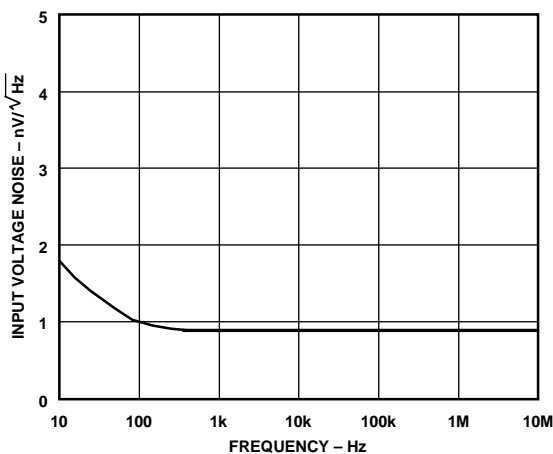
Ultrasound Preamplifiers

Seismic Detectors

$\Sigma\Delta$ ADC/DAC Buffers

PRODUCT DESCRIPTION

The AD797 is a very low noise, low distortion operational amplifier ideal for use as a preamplifier. The low noise of 0.9 nV/ $\sqrt{\text{Hz}}$ and low total harmonic distortion of -120 dB at audio bandwidths give the AD797 the wide dynamic range



AD797 Voltage Noise Spectral Density

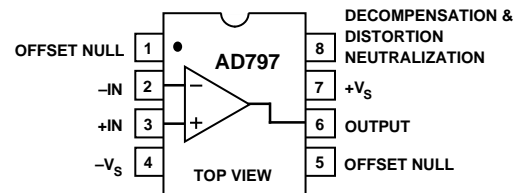
*Patent pending.

REV. C

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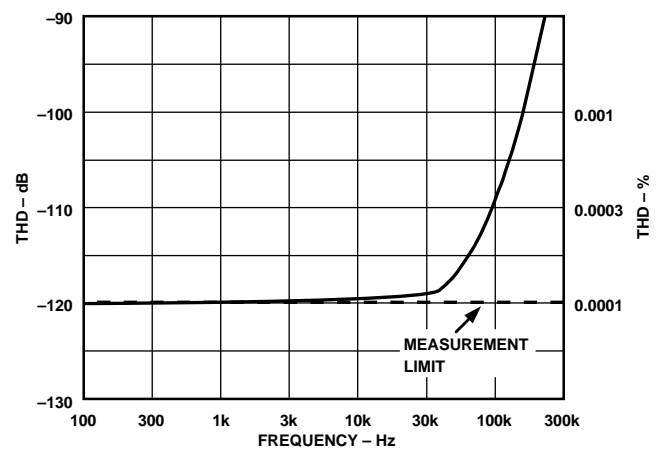
CONNECTION DIAGRAM

8-Pin Plastic Mini-DIP (N),
Cerdip (Q) and SOIC (R) Packages



necessary for preamps in microphones and mixing consoles. Furthermore, the AD797's excellent slew rate of 20 V/ μs and 110 MHz gain bandwidth make it highly suitable for low frequency ultrasound applications.

The AD797 is also useful in IR and Sonar Imaging applications where the widest dynamic range is necessary. The low distortion and 16-bit settling time of the AD797 make it ideal for buffering the inputs to $\Sigma\Delta$ ADCs or the outputs of high resolution DACs especially when they are used in critical applications such as seismic detection and spectrum analyzers. Key features such as a 50 mA output current drive and the specified power supply voltage range of ± 5 to ± 15 volts make the AD797 an excellent general purpose amplifier.



THD vs. Frequency

AD797–SPECIFICATIONS (@ T_A = +25°C and V_S = ±15 V dc, unless otherwise noted)

Model	Conditions	V _S	AD797A/S ¹			AD797B			Units	
			Min	Typ	Max	Min	Typ	Max		
INPUT OFFSET VOLTAGE Offset Voltage Drift	T _{MIN} to T _{MAX}	±5 V, ±15 V	25	80		10	40		μV	
		±5 V, ±15 V	50	125/180		30	60		μV	
INPUT BIAS CURRENT	T _{MIN} to T _{MAX}	±5 V, ±15 V	0.25	1.5		0.25	0.9		μA	
			0.5	3.0		0.25	2.0		μA	
INPUT OFFSET CURRENT	T _{MIN} to T _{MAX}	±5 V, ±15 V	100	400		80	200		nA	
			120	600/700		120	300		nA	
OPEN-LOOP GAIN	V _{OUT} = ±10 V R _{LOAD} = 2 kΩ T _{MIN} to T _{MAX} R _{LOAD} = 600 Ω T _{MIN} to T _{MAX} @ 20 kHz ²	±15 V								
			1	20		2	20		V/μV	
			1	6		2	10		V/μV	
			1	15		2	15		V/μV	
			1	5		2	7		V/μV	
			14000	20000		14000	20000		V/V	
DYNAMIC PERFORMANCE Gain Bandwidth Product -3 dB Bandwidth Full Power Bandwidth ³ Slew Rate Settling Time to 0.0015%	G = 1000 G = 1000 ² G = 10 V _O = 20 V p-p, R _{LOAD} = 1 kΩ R _{LOAD} = 1 kΩ 10 V Step	±15 V		110			110		MHz	
		±15 V		450			450		MHz	
		±15 V		8			8		MHz	
		±15 V		280			280		kHz	
		±15 V	12.5	20		12.5	20		V/μs	
				800	1200		800	1200	ns	
COMMON-MODE REJECTION	V _{CM} = CMVR T _{MIN} to T _{MAX}	±5 V, ±15 V	114	130		120	130		dB	
			110	120		114	120		dB	
POWER SUPPLY REJECTION	V _S = ±5 V to ±18 V T _{MIN} to T _{MAX}		114	130		120	130		dB	
			110	120		114	120		dB	
INPUT VOLTAGE NOISE	f = 0.1 Hz to 10 Hz f = 10 Hz f = 1 kHz f = 10 Hz–1 MHz	±15 V		50			50		nV p-p	
		±15 V		1.7			1.7	2.5	nV/√Hz	
		±15 V		0.9	1.2		0.9	1.2	nV/√Hz	
		±15 V		1.0	1.3		1.0	1.2	μV rms	
INPUT CURRENT NOISE	f = 1 kHz	±15 V		2.0			2.0		pA/√Hz	
INPUT COMMON-MODE VOLTAGE RANGE		±15 V	±11	±12		±11	±12		V	
		±5 V	±2.5	±3		±2.5	±3		V	
OUTPUT VOLTAGE SWING Short-Circuit Current Output Current ⁴	R _{LOAD} = 2 kΩ R _{LOAD} = 600 Ω R _{LOAD} = 600 Ω	±15 V	±12	±13		±12	±13		V	
		±15 V	±11	±13		±11	±13		V	
		±5 V	±2.5	±3		±2.5	±3		V	
		±5 V, ±15 V		80			80		mA	
		±5 V, ±15 V	30	50		30	50		mA	
TOTAL HARMONIC DISTORTION	R _{LOAD} = 1 kΩ, C _N = 50 pF f = 250 kHz, 3 V rms R _{LOAD} = 1 kΩ f = 20 kHz, 3 V rms	±15 V		-98	-90		-98	-90	dB	
		±15 V		-120	-110		-120	-110	dB	
INPUT CHARACTERISTICS Input Resistance (Differential) Input Resistance (Common Mode) Input Capacitance (Differential) ⁵ Input Capacitance (Common Mode)				7.5			7.5		kΩ	
				100			100		MΩ	
				20			20		pF	
				5			5		pF	
OUTPUT RESISTANCE	A _V = +1, f = 1 kHz			3			3		mΩ	
POWER SUPPLY Operating Range Quiescent Current			±5		±18		±5		±18	V
		±5 V, ±15 V		8.2	10.5		8.2	10.5		mA

NOTES

¹See standard military drawing for 883B specifications.

²Specified using external decompensation capacitor, see Applications section.

³Full Power Bandwidth = Slew Rate/2 π V_{PEAK}.

⁴Output Current for |V_S - V_{OUT}| > 4 V, A_{OL} > 200 kΩ.

⁵Differential input capacitance consists of 1.5 pF package capacitance and 18.5 pF from the input differential pair.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS¹

Supply Voltage	±18 V
Internal Power Dissipation @ +25°C ²	
Input Voltage	±V _S
Differential Input Voltage ³	±0.7 V
Output Short Circuit Duration	Indefinite Within max Internal Power Dissipation
Storage Temperature Range (Cerdip)	-65°C to +150°C
Storage Temperature Range (N, R Suffix)	-65°C to +125°C
Operating Temperature Range	
AD797A/B	-40°C to +85°C
AD797S	-55°C to +125°C
Lead Temperature Range (Soldering 60 sec)	+300°C

NOTES

¹Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

²Internal Power Dissipation:

8-Pin SOIC = 0.9 Watts (T_A-25°C)/θ_{JA}

8-Pin Plastic DIP and Cerdip = 1.3 Watts - (T_A-25°C)/θ_{JA}

Thermal Characteristics

8-Pin Plastic DIP Package: θ_{JA} = 95°C/W

8-Pin Cerdip Package: θ_{JA} = 110°C/W

8-Pin Small Outline Package: θ_{JA} = 155°C/W

³The AD797's inputs are protected by back-to-back diodes. To achieve low noise, internal current limiting resistors are not incorporated into the design of this amplifier. If the differential input voltage exceeds ±0.7 V, the input current should be limited to less than 25 mA by series protection resistors. Note, however, that this will degrade the low noise performance of the device.

ESD SUSCEPTIBILITY

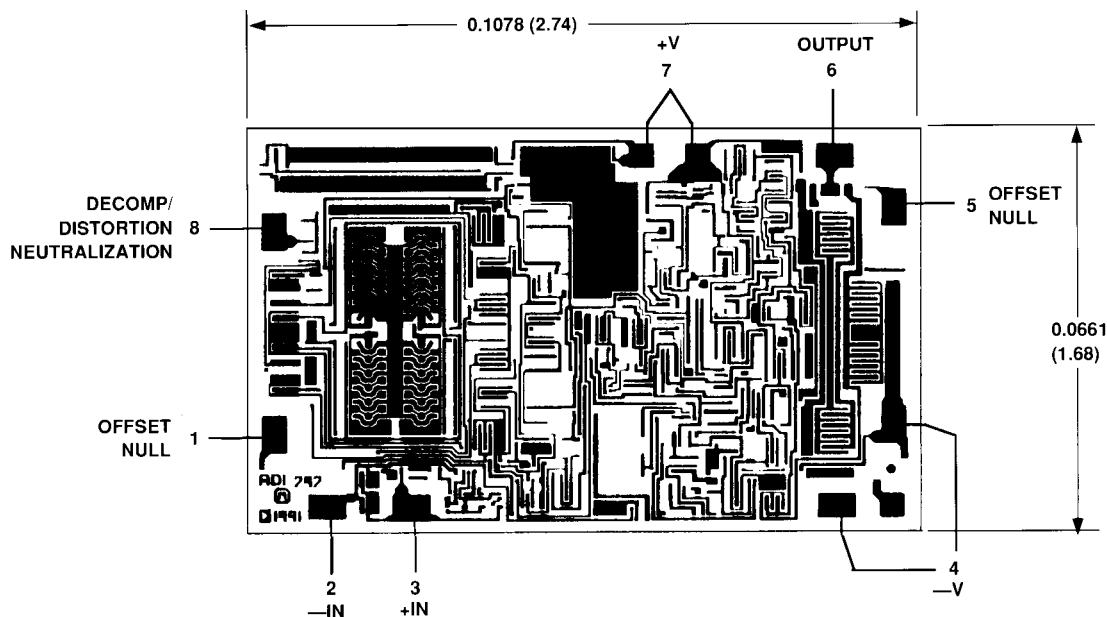
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 volts, which readily accumulate on the human body and on test equipment, can discharge without detection. Although the AD797 features proprietary ESD protection circuitry, permanent damage may still occur on these devices if they are subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid any performance degradation or loss of functionality.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD797AN	-40°C to +85°C	8-Pin Plastic DIP	N-8
AD797BN	-40°C to +85°C	8-Pin Plastic DIP	N-8
AD797BR	-40°C to +85°C	8-Pin Plastic SOIC	SO-8
AD797BR-REEL	-40°C to +85°C	8-Pin Plastic SOIC	SO-8
AD797BR-REEL7	-40°C to +85°C	8-Pin Plastic SOIC	SO-8
AD797AR	-40°C to +85°C	8-Pin Plastic SOIC	SO-8
AD797AR-REEL	-40°C to +85°C	8-Pin Plastic SOIC	SO-8
AD797AR-REEL7	-40°C to +85°C	8-Pin Plastic SOIC	SO-8
5962-9313301MPA	-55°C to +125°C	8-Pin Cerdip	Q-8

METALIZATION PHOTO

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



NOTE

The AD797 has double layer metal. Only one layer is shown here for clarity.

AD797—Typical Characteristics

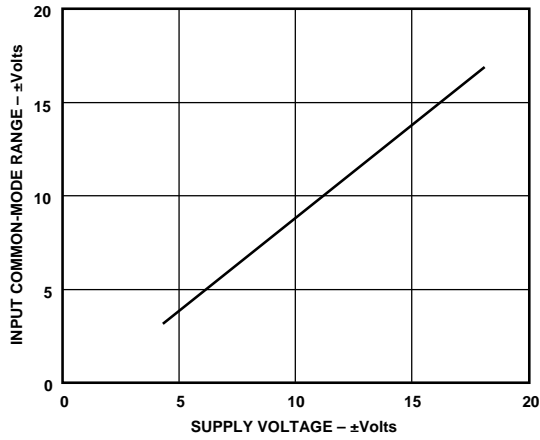


Figure 1. Common-Mode Voltage Range vs. Supply

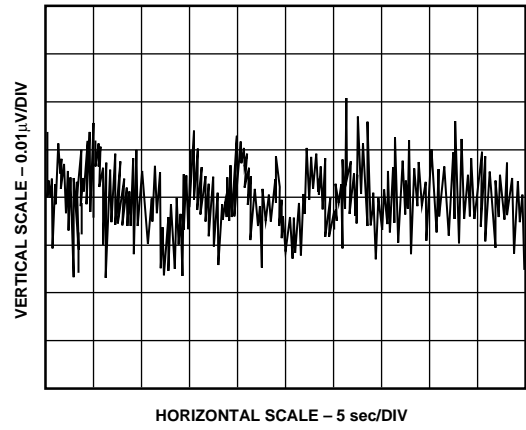


Figure 4. 0.1 Hz to 10 Hz Noise

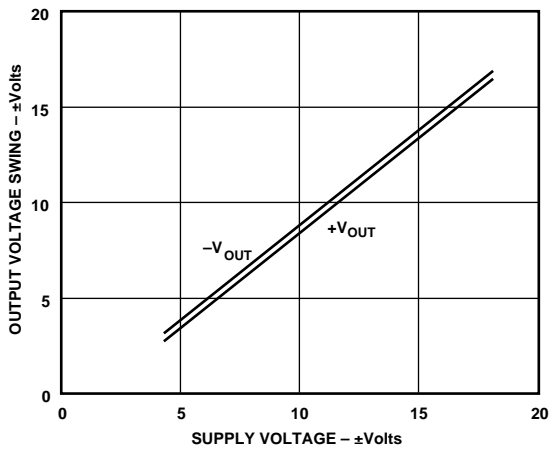


Figure 2. Output Voltage Swing vs. Supply

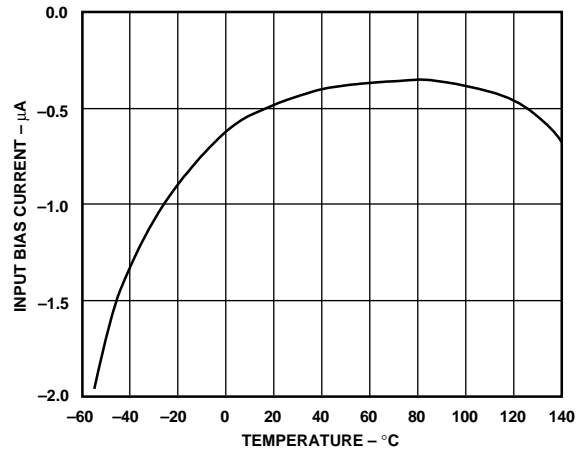


Figure 5. Input Bias Current vs. Temperature

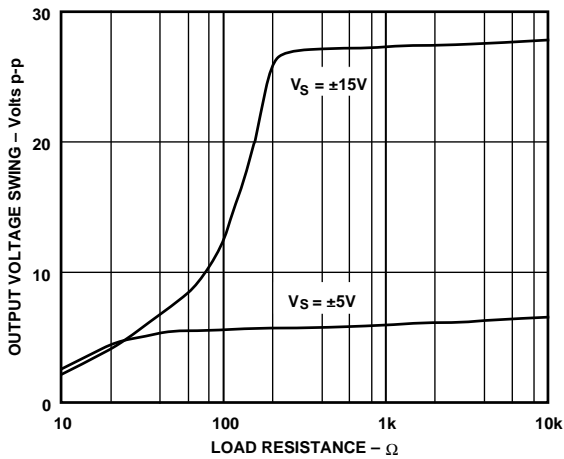


Figure 3. Output Voltage Swing vs. Load Resistance

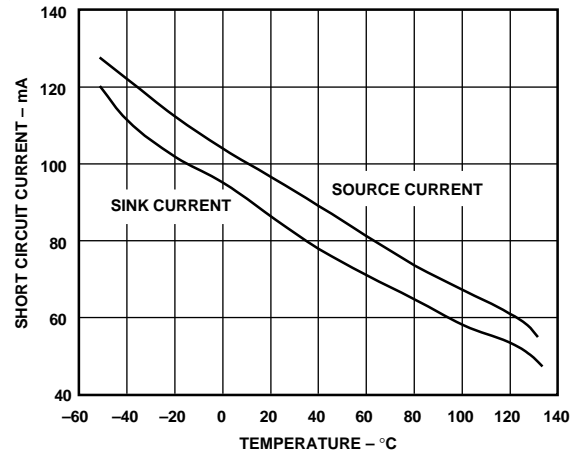


Figure 6. Short Circuit Current vs. Temperature

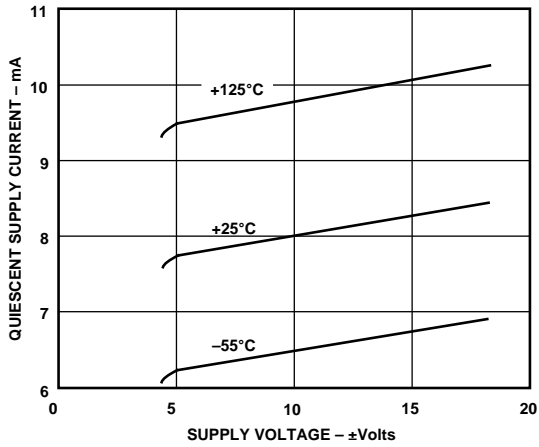


Figure 7. Quiescent Supply Current vs. Supply Voltage

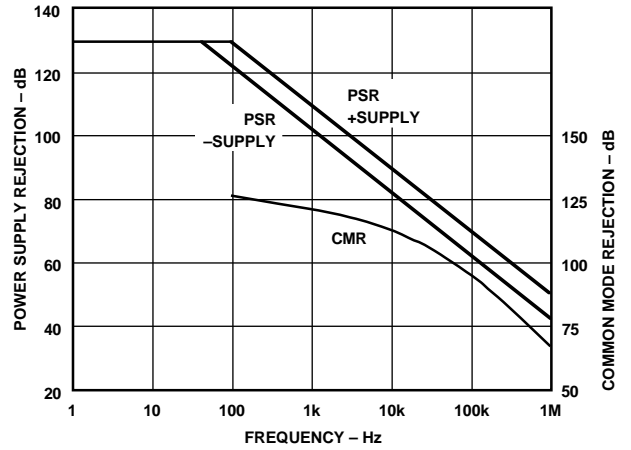


Figure 10. Power Supply and Common-Mode Rejection vs. Frequency

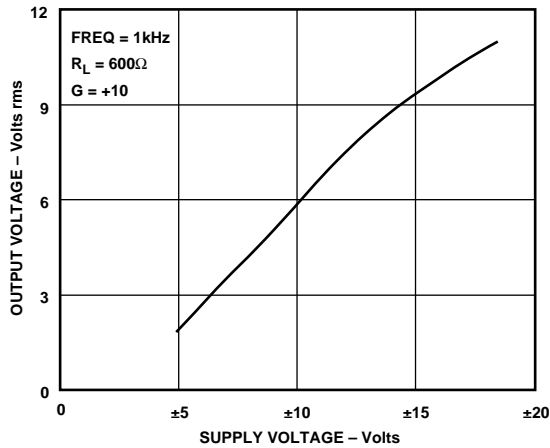


Figure 8. Output Voltage vs. Supply for 0.01% Distortion

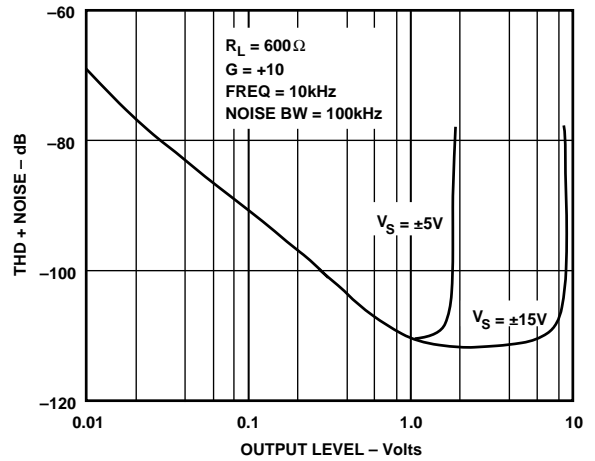


Figure 11. Total Harmonic Distortion (THD) + Noise vs. Output Level

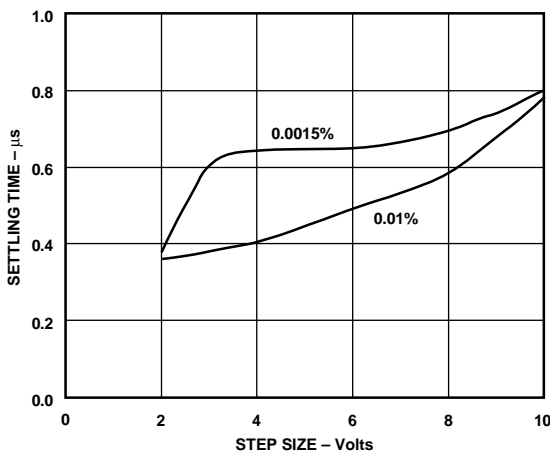


Figure 9. Settling Time vs. Step Size (±)

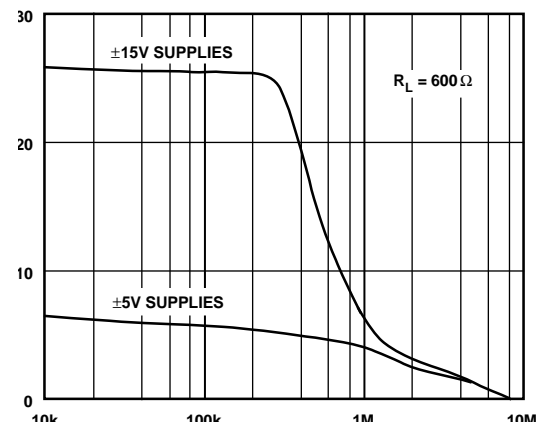


Figure 12. Large Signal Frequency Response

AD797—Typical Characteristics

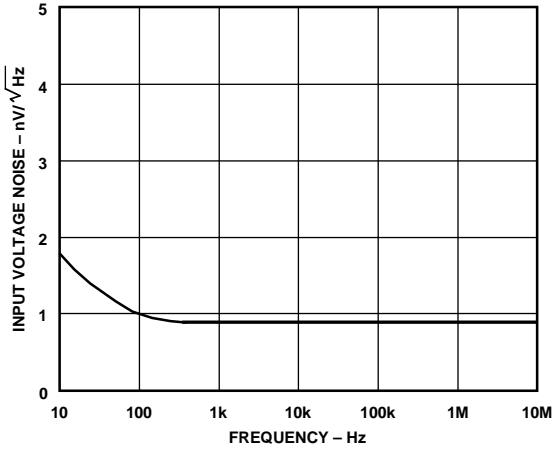


Figure 13. Input Voltage Noise Spectral Density

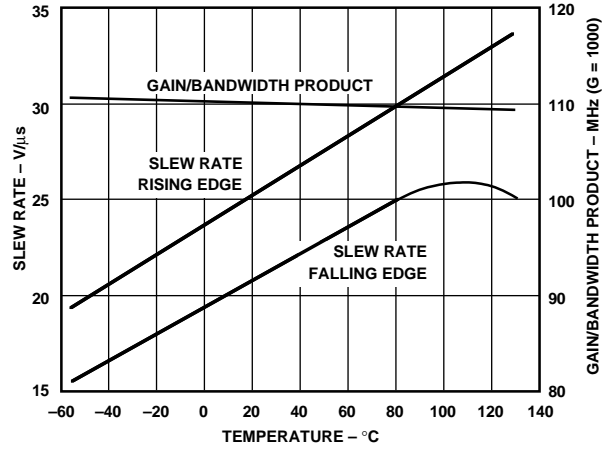


Figure 16. Slew Rate & Gain/Bandwidth Product vs. Temperature

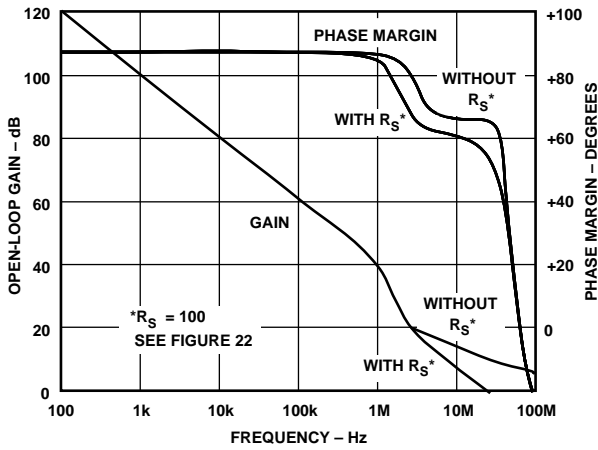


Figure 14. Open-Loop Gain & Phase vs. Frequency

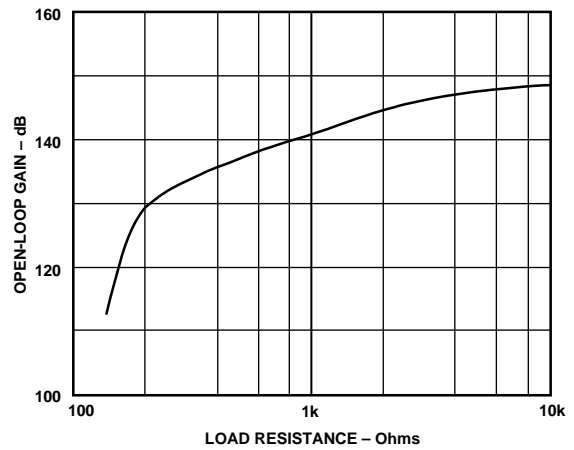


Figure 17. Open-Loop Gain vs. Resistive Load

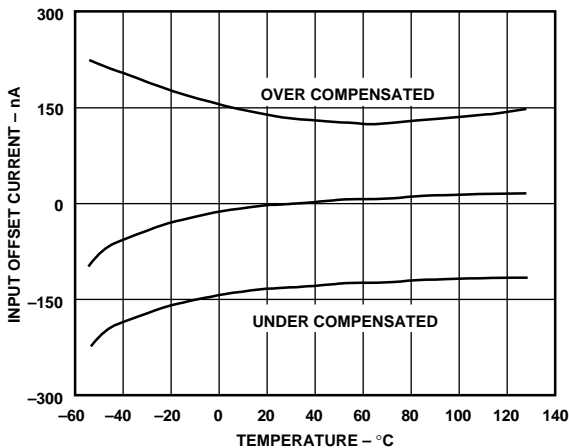


Figure 15. Input Offset Current vs. Temperature

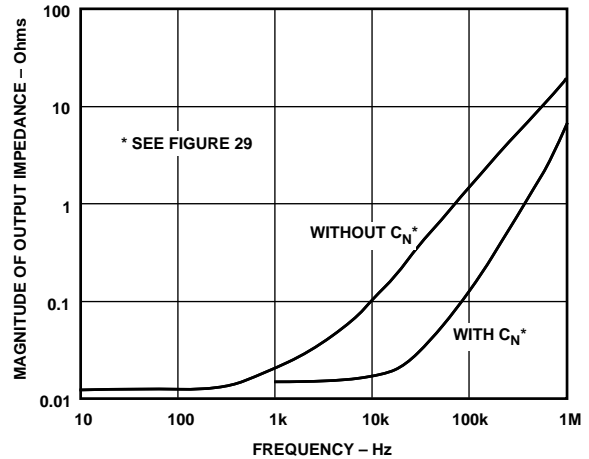
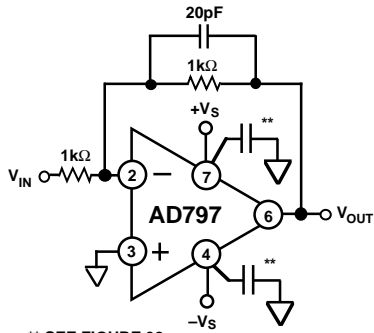


Figure 18. Magnitude of Output Impedance vs. Frequency



** SEE FIGURE 32

Figure 19. Inverter Connection

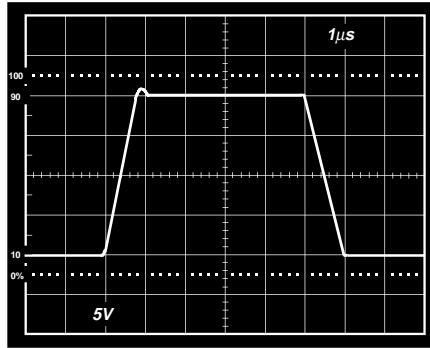


Figure 20. Inverter Large Signal Pulse Response

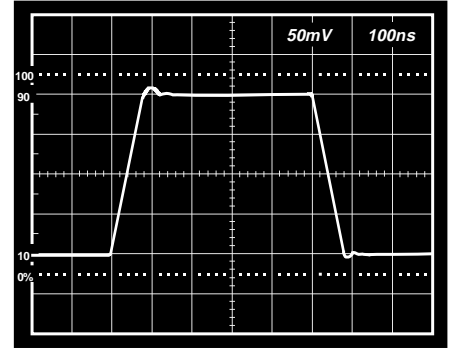
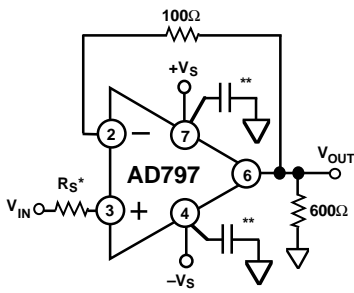


Figure 21. Inverter Small Signal Pulse Response



* VALUE OF SOURCE RESISTANCE - SEE TEXT
** SEE FIGURE 32

Figure 22. Follower Connection

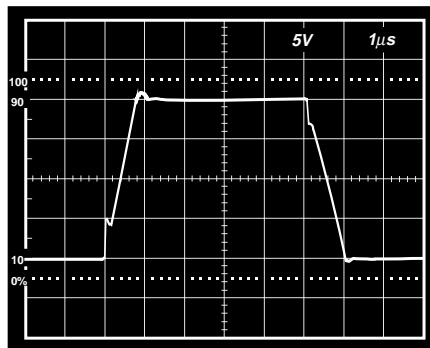


Figure 23. Follower Large Signal Pulse Response

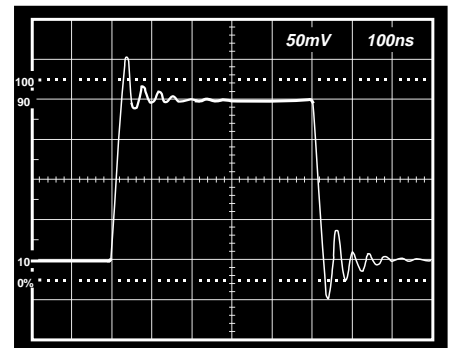


Figure 24. Follower Small Signal Pulse Response

See Figure 40 for settling time test circuit.

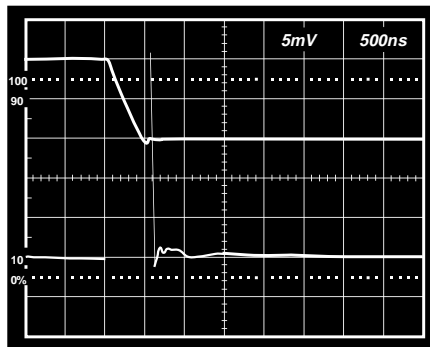


Figure 25. 16-Bit Settling Time Positive Input Pulse

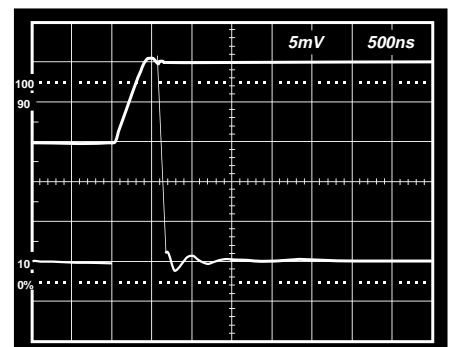
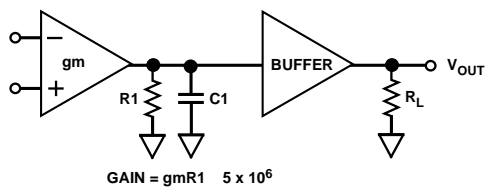


Figure 26. 16-Bit Settling Time Negative Input Pulse

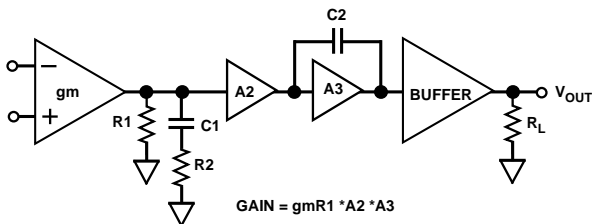
AD797

THEORY OF OPERATION

The new architecture of the AD797 was developed to overcome inherent limitations in previous amplifier designs. Previous precision amplifiers used three stages to ensure high open-loop gain, Figure 27b, at the expense of additional frequency compensation components. Slew rate and settling performance are usually compromised, and dynamic performance is not adequate beyond audio frequencies. As can be seen in Figure 27b, the first stage gain is rolled off at high frequencies by the compensation network. Second stage noise and distortion will then appear at the input and degrade performance. The AD797 on the other hand, uses a single ultrahigh gain stage to achieve dc as well as dynamic precision. As shown in the simplified schematic (Figure 28), nodes A, B, and C all track in voltage forcing the operating points of all pairs of devices in the signal path to match. By exploiting the inherent matching of devices fabricated on the same IC chip, high open-loop gain, CMRR, PSRR, and low V_{OS} are all guaranteed by pairwise device *matching* (i.e., NPN to NPN & PNP to PNP), and not absolute parameters such as beta and early voltage.



a.



b.

Figure 27. Model of AD797 vs. That of a Typical Three-Stage Amplifier

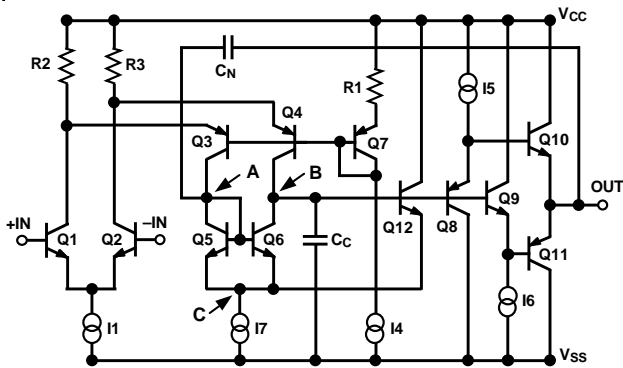


Figure 28. AD797 Simplified Schematic

This matching benefits not just dc precision but since it holds up dynamically, both distortion and settling time are also reduced. This single stage has a voltage gain of $>5 \times 10^6$ and $V_{OS} < 80 \mu V$, while at the same time providing THD + noise of less than -120 dB and true 16 bit settling in less than 800 ns. The elimination of second stage noise effects has the additional benefit of making the low noise of the AD797 (< 0.9 nV/ \sqrt{Hz}) extend to beyond 1 MHz. This means new levels of performance for sampled data and imaging systems. All of this performance as well as load drive in excess of 30 mA are made possible by Analog Devices' advanced Complementary Bipolar (CB) process.

Another unique feature of this circuit is that the addition of a single capacitor, C_N (Figure 28), enables cancellation of distortion due to the output stage. This can best be explained by referring to a simplified representation of the AD797 using idealized blocks for the different circuit elements (Figure 29).

A single equation yields the open-loop transfer function of this amplifier, solving it (at Node B) yields:

$$\frac{V_O}{V_{IN}} = \frac{gm}{\frac{C_N}{A} j\omega - C_N j\omega - \frac{C_C}{A} j\omega}$$

gm = the transconductance of Q1 and Q2

A = the gain of the output stage, (~ -1)

V_O = voltage at the output

V_{IN} = differential input voltage

When C_N is equal to C_C this gives the ideal single pole op amp response:

$$\frac{V_O}{V_{IN}} = \frac{gm}{j\omega C}$$

The terms in A, which include the properties of the output stage such as output impedance and distortion, cancel by simple subtraction, and therefore the distortion cancellation does not affect the stability or frequency response of the amplifier. With only 500 μA of output stage bias the AD797 delivers a 1 kHz sine wave into 600 Ω at 7 V rms with only 1 ppm of distortion.

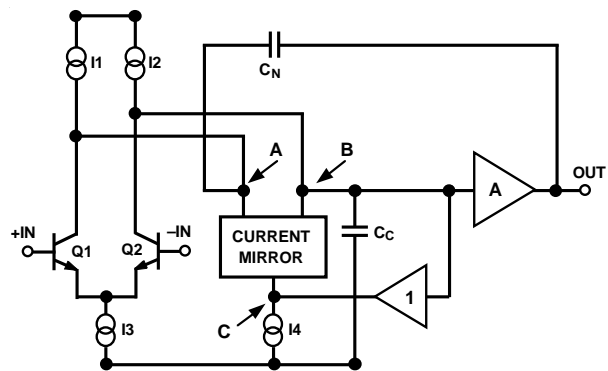


Figure 29. AD797 Block Diagram

NOISE AND SOURCE IMPEDANCE CONSIDERATIONS

The AD797's ultralow voltage noise of $0.9 \text{ nV}/\sqrt{\text{Hz}}$ is achieved with special input transistors running at nearly 1 mA of collector current. It is important then to consider the total input referred noise (e_{Ntotal}), which includes contributions from voltage noise (e_N), current noise (i_N), and resistor noise ($\sqrt{4kTr_S}$).

$$e_{Ntotal} = [e_N^2 + 4kTr_S + 4(i_N r_S)^2]^{1/2} \quad \text{Equation 1}$$

where r_S = total input source resistance.

This equation is plotted for the AD797 in Figure 30. Since optimum dc performance is obtained with matched source resistances, this case is considered even though it is clear from Equation 1 that eliminating the balancing source resistance will lower the total noise by reducing the total r_S by a factor of two.

At very low source resistance ($r_S < 50 \Omega$), the amplifiers' voltage noise dominates. As source resistance increases the Johnson noise of r_S dominates until at higher resistances ($r_S > 2 \text{ k}\Omega$) the current noise component is larger than the resistor noise.

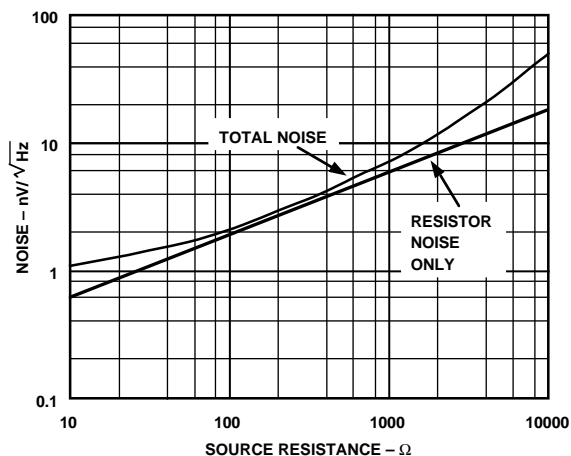


Figure 30. Noise vs. Source Resistance

The AD797 is the optimum choice for low noise performance provided the source resistance is kept $< 1 \text{ k}\Omega$. At higher values of source resistance, optimum performance with respect to noise alone is obtained with other amplifiers from Analog Devices (see Table I).

Table I. Recommended Amplifiers for Different Source Impedances

r_S , ohms	Recommended Amplifier
0 to $< 1 \text{ k}$	AD797
1 k to $< 10 \text{ k}$	AD707, AD743/AD745, OP27/OP37, OP07
10 k to $< 100 \text{ k}$	AD705, AD743/AD745, OP07
$> 100 \text{ k}$	AD548, AD549, AD645, AD711, AD743/AD745

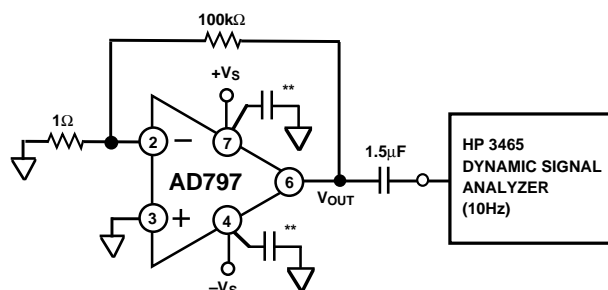
LOW FREQUENCY NOISE

Analog Devices specifies low frequency noise as a peak to peak (p-p) quantity in a 0.1 Hz to 10 Hz bandwidth. Several techniques can be used to make this measurement. The usual technique involves amplifying, filtering, and measuring the amplifiers noise for a predetermined test time. The noise bandwidth of the filter is corrected for and the test time is carefully controlled since the measurement time acts as an additional low frequency roll-off.

The plot in Figure 4 was made using a slightly different technique. Here an FFT based instrument (Figure 31) is used to generate a 10 Hz "brickwall" filter. A low frequency pole at 0.1 Hz is generated with an external ac coupling capacitor, the instrument being dc coupled.

Several precautions are necessary to get optimum low frequency noise performance:

1. Care must be used to account for the effects of r_S , even a 10Ω resistor has $0.4 \text{ nV}/\sqrt{\text{Hz}}$ of noise (an error of 9% when root sum squared with $0.9 \text{ nV}/\sqrt{\text{Hz}}$).
2. The test set up must be fully warmed up to prevent e_{OS} drift from erroneously contributing to input noise.
3. Circuitry must be shielded from air currents. Heat flow out of the package through its leads creates the opportunity for a thermoelectric potential at every junction of different metals. Selective heating and cooling of these by random air currents will appear as $1/f$ noise and obscure the true device noise.
4. The results must be interpreted using valid statistical techniques.



** USE POWER SUPPLY BYPASSING SHOWN IN FIGURE 32.

Figure 31. Test Setup for Measuring 0.1 Hz to 10 Hz Noise

WIDEBAND NOISE

The AD797, due to its single stage design, has the property that its noise is flat over frequencies from less than 10 Hz to beyond 1 MHz . This is not true of most dc precision amplifiers where second stage noise contributes to input referred noise beyond the audio frequency range. The AD797 offers new levels of performance in wideband imaging applications. In sampled data systems, where aliasing of out of band noise into the signal band is a problem, the AD797 will out perform all previously available IC op amps.

AD797

BYPASSING CONSIDERATIONS

To take full advantage of the very wide bandwidth and dynamic range capabilities of the AD797 requires some precautions. First, multiple bypassing is recommended in any precision application. A 1.0 μF –4.7 μF tantalum in parallel with 0.1 μF ceramic bypass capacitors are sufficient in most applications. When driving heavy loads a larger demand is placed on the supply bypassing. In this case selective use of larger values of tantalum capacitors and damping of their lead inductance with small value (1.1 Ω to 4.7 Ω) carbon resistors can be an improvement. Figure 32 summarizes bypassing recommendations. The symbol (**) is used throughout this data sheet to represent the parallel combination of a 0.1 μF and a 4.7 μF capacitor.

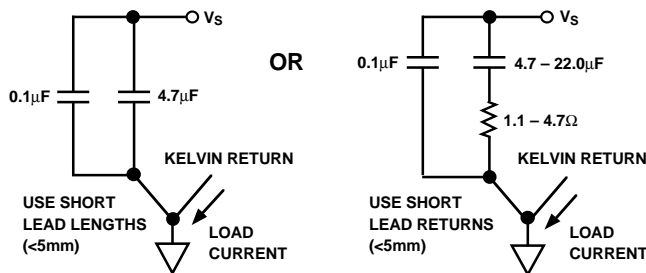
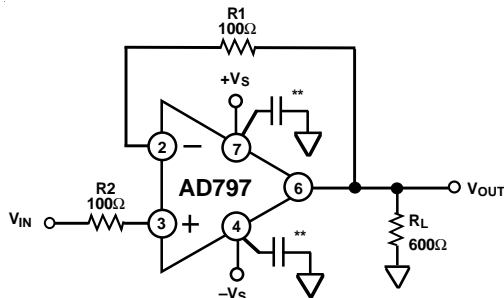


Figure 32. Recommended Power Supply Bypassing

THE NONINVERTING CONFIGURATION

Ultralow noise requires very low values of r_{BB} (the internal parasitic resistance) for the input transistors ($\approx 6 \Omega$). This implies very little damping of input and output reactive interactions. With the AD797, additional input series damping is required for stability with direct input to output feedback. A 100 Ω resistor in the inverting input (Figure 33) is sufficient; the 100 Ω balancing resistor (R2) is recommended, but is not required for stability. The noise penalty is minimal ($e_{\text{N total}} \approx 2.1 \text{ nV}/\sqrt{\text{Hz}}$), which is usually insignificant. Best response flatness is obtained with the addition of a small capacitor ($C_{\text{L}} < 33 \text{ pF}$) in parallel with the 100 Ω resistor (Figure 34). The input source resistance and capacitance will also affect the response slightly and experimentation may be necessary for best results.



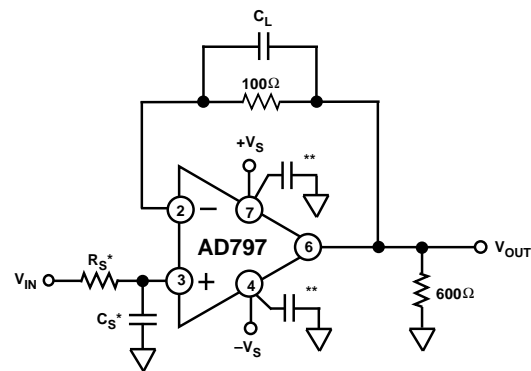
** USE POWER SUPPLY BYPASSING SHOWN IN FIGURE 32.

Figure 33. Voltage Follower Connection

Low noise preamplification is usually done in the noninverting mode (Figure 35). For lowest noise the equivalent resistance of the feedback network should be as low as possible. The 30 mA minimum drive current of the AD797 makes it easier to achieve this. The feedback resistors can be made as low as possible with due consideration to load drive and power consumption. Table II gives some representative values for the AD797 as a low noise

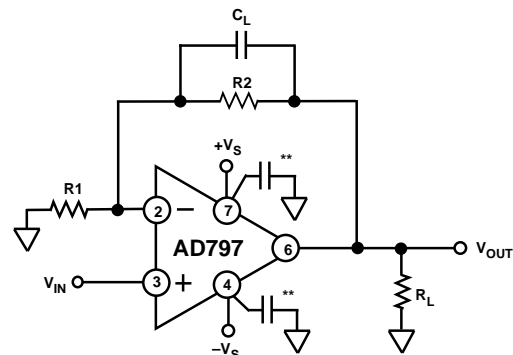
follower. Operation on 5 volt supplies allows the use of a 100 Ω or less feedback network ($R_1 + R_2$). Since the AD797 shows no unusual behavior when operating near its maximum rated current, it is suitable for driving the AD600/AD602 (Figure 47) while preserving their low noise performance.

Optimum flatness and stability at noise gains >1 sometimes requires a small capacitor (C_{L}) connected across the feedback resistor (R_1 , Figure 35). Table II includes recommended values of C_{L} for several gains. In general, when R_2 is greater than 100 Ω and C_{L} is greater than 33 pF, a 100 Ω resistor should be placed in series with C_{L} . Source resistance matching is assumed, and the AD797 should never be operated with unbalanced source resistance $>200 \text{ k}\Omega/\text{G}$.



* SEE TEXT
** USE POWER SUPPLY BYPASSING SHOWN IN FIGURE 32.

Figure 34. Alternative Voltage Follower Connection



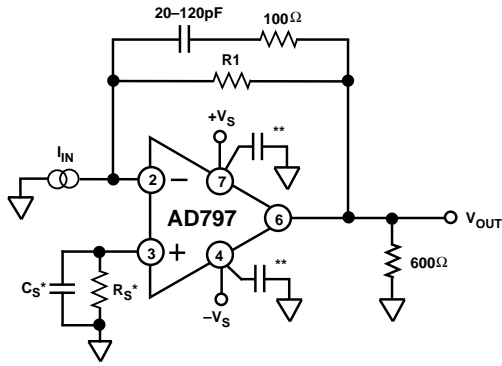
** USE POWER SUPPLY BYPASSING SHOWN IN FIGURE 32.

Figure 35. Low Noise Preamplifier

Table II. Values for Follower With Gain Circuit

Gain	R1	R2	C_{L}	Noise (Excluding r_{s})
2	1 k Ω	1 k Ω	$\approx 20 \text{ pF}$	3.0 nV/ $\sqrt{\text{Hz}}$
2	300 Ω	300 Ω	$\approx 10 \text{ pF}$	1.8 nV/ $\sqrt{\text{Hz}}$
10	33.2 Ω	300 Ω	$\approx 5 \text{ pF}$	1.2 nV/ $\sqrt{\text{Hz}}$
20	16.5 Ω	316 Ω		1.0 nV/ $\sqrt{\text{Hz}}$
>35	10 Ω	$(\text{G}-1) \cdot 10 \Omega$		0.98 nV/ $\sqrt{\text{Hz}}$

The I-to-V converter is a special case of the follower configuration. When the AD797 is used in an I-to-V converter, for instance as a DAC buffer, the circuit of Figure 36 should be used. The value of C_{L} depends on the DAC and again, if C_{L} is



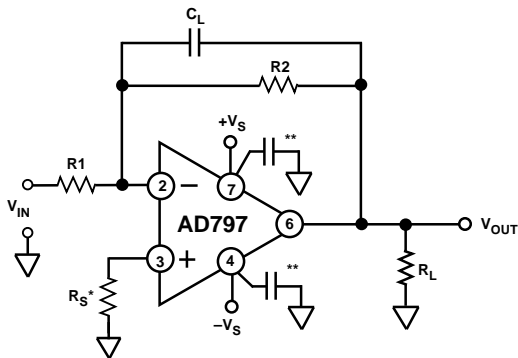
* SEE TEXT
 ** USE POWER SUPPLY BYPASSING SHOWN IN FIGURE 32.

Figure 36. I-to-V Converter Connection

greater than 33 pF a 100 Ω series resistor is required. A bypassed balancing resistor (R_S and C_S) can be included to minimize dc errors.

THE INVERTING CONFIGURATION

The inverting configuration (Figure 37) presents a low input impedance, R_1 , to the source. For this reason, the goals of both low noise and input buffering are at odds with one another. Nonetheless, the excellent dynamics of the AD797 will make it the preferred choice in many inverting applications, and with careful selection of feedback resistors the noise penalties will be minimal. Some examples are presented in Table II and Figure 37.



* SEE TEXT
 ** USE POWER SUPPLY BYPASSING SHOWN IN FIGURE 32.

Figure 37. Inverting Amplifier Connection

Table III. Values for Inverting Circuit

Gain	R1	R2	C _L	Noise (Excluding r _s)
-1	1 kΩ	1 kΩ	≈20 pF	3.0 nV/√Hz
-1	300 Ω	300 Ω	≈10 pF	1.8 nV/√Hz
-10	150 Ω	1500 Ω	≈5 pF	1.8 nV/√Hz

DRIVING CAPACITIVE LOADS

The capacitive load driving capabilities of the AD797 are displayed in Figure 38. At gains over 10 usually no special precautions are necessary. If more drive is desirable the circuit in Figure 39 should be used. Here a 5000 pF load can be driven cleanly at any noise gain ≥ 2.

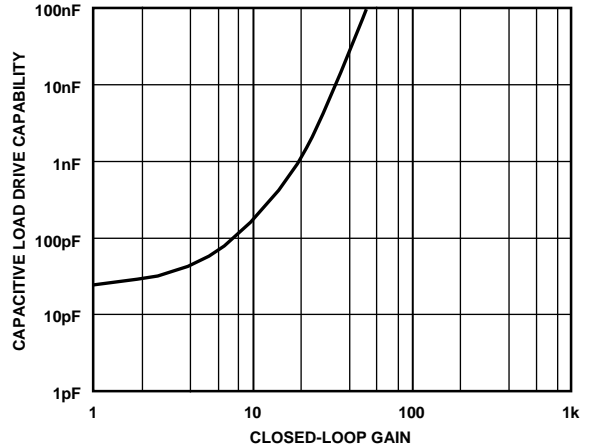
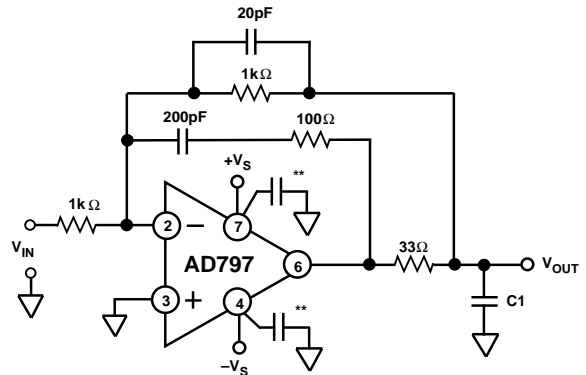


Figure 38. Capacitive Load Drive Capability vs. Closed Loop Gain



** USE POWER SUPPLY BYPASSING SHOWN IN FIGURE 32.

Figure 39. Recommended Circuit for Driving a High Capacitance Load

SETTLING TIME

The AD797 is unique among ultralow noise amplifiers in that it settles to 16 bits (<150 μV) in less than 800 ns. Measuring this performance presents a challenge. A special test setup (Figure 40) was developed for this purpose. The input signal was obtained from a resonant reed switch pulse generator, available from Tektronix as calibration Fixture No. 067-0608-00. When open, the switch is simply 50 Ω to ground and settling is purely a passive pulse decay and inherently flat. The low repetition rate signal was captured on a digital oscilloscope after being amplified and clamped twice. The selection of plug-in for the oscilloscope was made for minimum overload recovery.

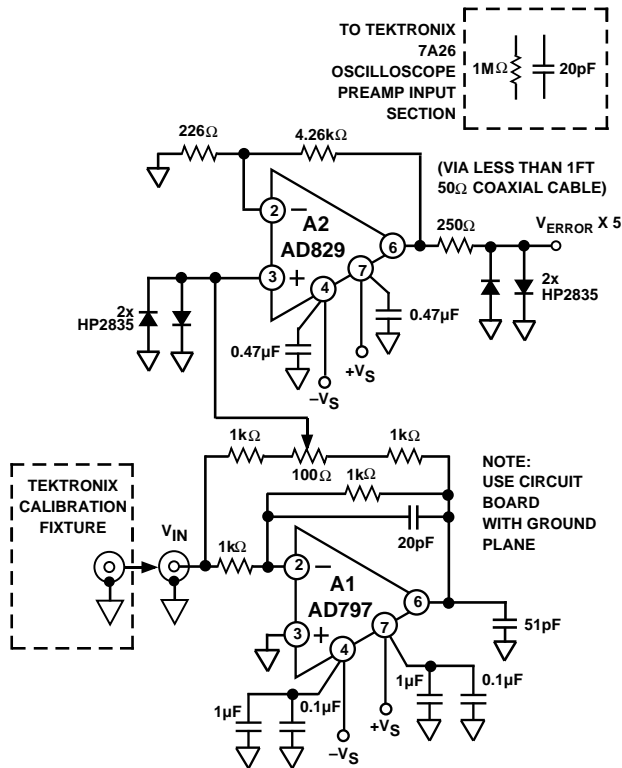


Figure 40. Settling Time Test Circuit

DISTORTION REDUCTION

The AD797 has distortion performance (THD < -120 dB, @ 20 kHz, 3 V rms, $R_L = 600 \Omega$) unequaled by most voltage feedback amplifiers.

At higher gains and higher frequencies THD will increase due to reduction in loop gain. However in contrast to most conventional voltage feedback amplifiers the AD797 provides two effective means of reducing distortion, as gain and frequency are increased; cancellation of the output stage's distortion and gain bandwidth enhancement by decompensation. By applying these techniques gain bandwidth can be increased to 450 MHz at $G = 1000$ and distortion can be held to -100 dB at 20 kHz for $G = 100$.

The unique design of the AD797 provides for cancellation of the output stage's distortion (patent pending). To achieve this a capacitance equal to the effective compensation capacitance, usually 50 pF, is connected between Pin 8 and the output (C2 in Figure 41). Use of this feature will improve distortion performance when the closed loop gain is more than 10 or when frequencies of interest are greater than 30 kHz.

Bandwidth enhancement via decompensation is achieved by connecting a capacitor from Pin 8 to ground (C1 in Figure 41) effectively subtracting from the value of the internal compensation capacitance (50 pF), yielding a smaller effective compensation capacitance and, therefore, a larger bandwidth. The benefits of this begin at closed loop gains of 100 and up. A maximum value of ≈ 33 pF at gains of 1000 and up is recommended. At a gain of 1000 the bandwidth is 450 kHz.

Table IV and Figure 42 summarize the performance of the AD797 with distortion cancellation and decompensation.

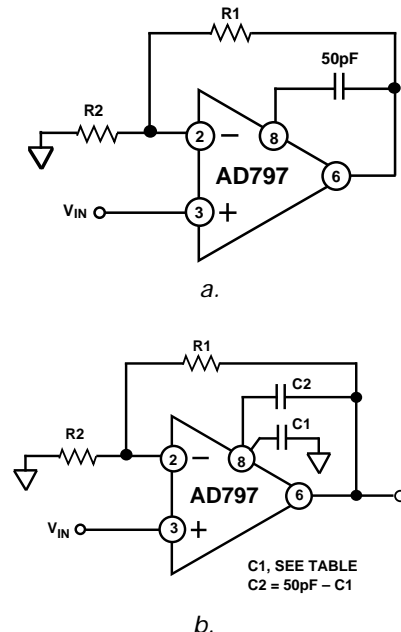


Figure 41. Recommended Connections for Distortion Cancellation and Bandwidth Enhancement

Table IV. Recommended External Compensation

	A/B		A			B		
	R1 Ω	R2 Ω	C1 (pF)	C2 (pF)	3 dB BW	C1 (pF)	C2 (pF)	3 dB BW
$G = 10$	909	100	0	50	6 MHz	0	50	6 MHz
$G = 100$	1 k	10	0	50	1 MHz	15	33	1.5 MHz
$G = 1000$	10 k	10	0	50	110 kHz	33	15	450 kHz

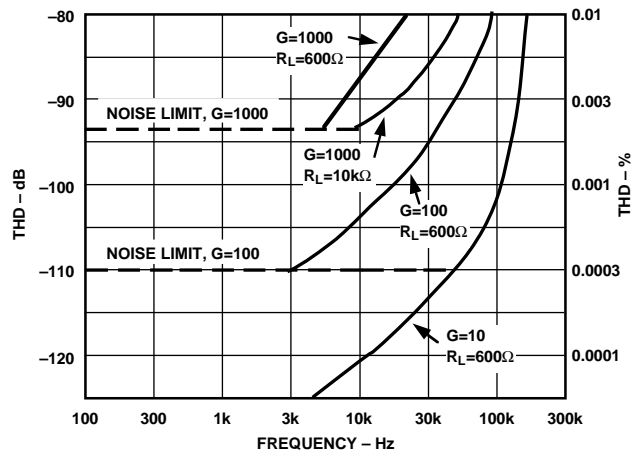


Figure 42. Total Harmonic Distortion (THD) vs. Frequency @ 3 V rms for Figure 41b

Differential Line Receiver

The differential receiver circuit of Figure 43 is useful for many applications from audio to MRI imaging. It allows extraction of a low level signal in the presence of common-mode noise. As shown in Figure 44, the AD797 provides this function with only 9 nV/ $\sqrt{\text{Hz}}$ noise at the output. Figure 45 shows the AD797's 20-bit THD performance over the audio band and 16-bit accuracy to 250 kHz.

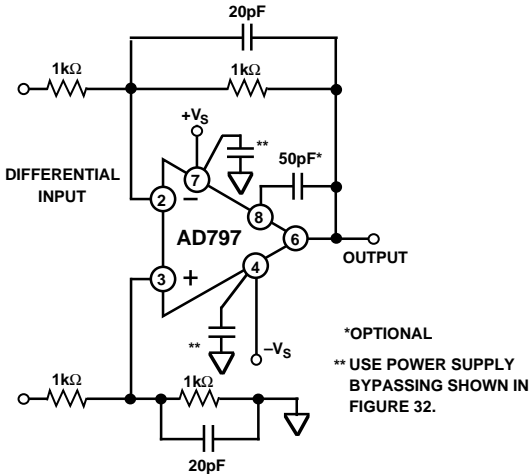


Figure 43. Differential Line Receiver

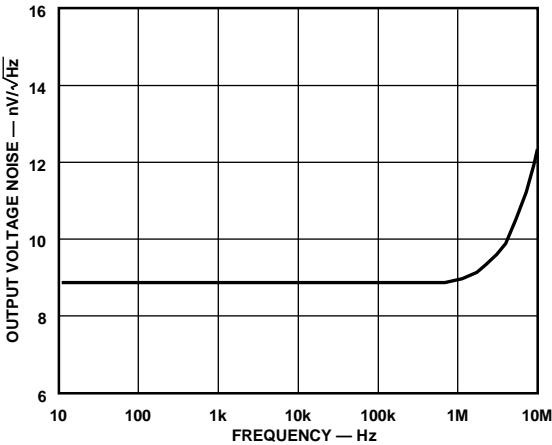


Figure 44. Output Voltage Noise Spectral Density for Differential Line Receiver

A General Purpose ATE/Instrumentation Input/Output Driver

The ultralow noise and distortion of the AD797 may be combined with the wide bandwidth, slew rate, and load drive of a current feedback amplifier to yield a very wide dynamic range general purpose driver. The circuit of Figure 46 combines the AD797 with the AD811 in just such an application. Using the

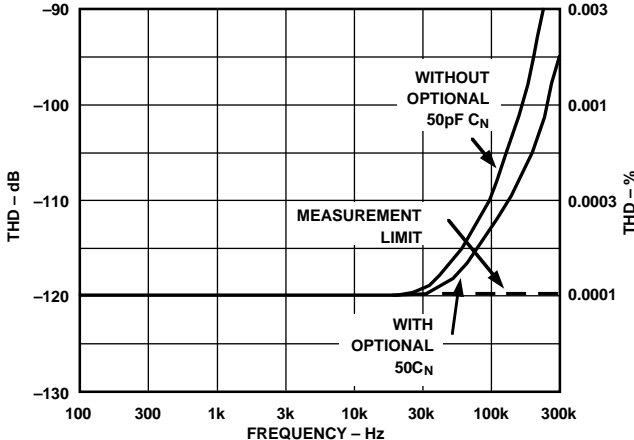


Figure 45. Total Harmonic Distortion (THD) vs. Frequency for Differential Line Receiver

component values shown, this circuit is capable of better than -90 dB THD with a ± 5 V, 500 kHz output signal. The circuit is therefore suitable for driving high resolution A/D converters and as an output driver in automatic test equipment (ATE) systems. Using a 100 kHz sine wave, the circuit will drive a 600 Ω load to a level of 7 V rms with less than -109 dB THD, and a 10 k Ω load at less than -117 dB THD.

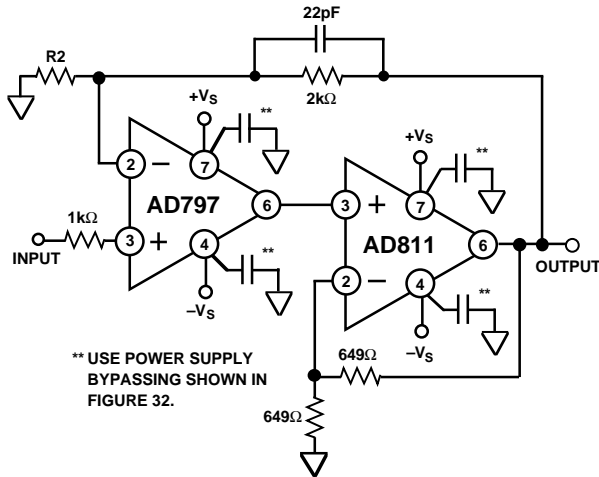


Figure 46. A General Purpose ATE/Instrumentation Input/Output Driver

AD797

Ultrasound/Sonar Imaging Preamp

The AD600 variable gain amplifier provides the time controlled gain (TCG) function necessary for very wide dynamic range sonar and low frequency ultrasound applications. Under some circumstances, it is necessary to buffer the input of the AD600 to preserve its low noise performance. To optimize dynamic range this buffer should have at most 6 dB of gain. The combination of low noise and low gain is difficult to achieve. The input buffer circuit shown in Figure 47 provides 1 nV/ $\sqrt{\text{Hz}}$ noise performance at a gain of two (dc to 1 MHz) by using 26.1 Ω resistors in its feedback path. Distortion is only -50 dBc @ 1 MHz at a 2 volt p-p output level and drops rapidly to better than -70 dBc at an output level of 200 mV p-p.

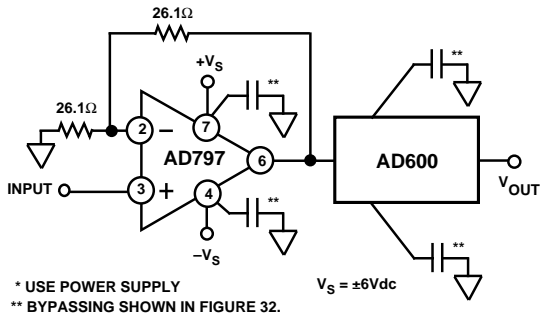
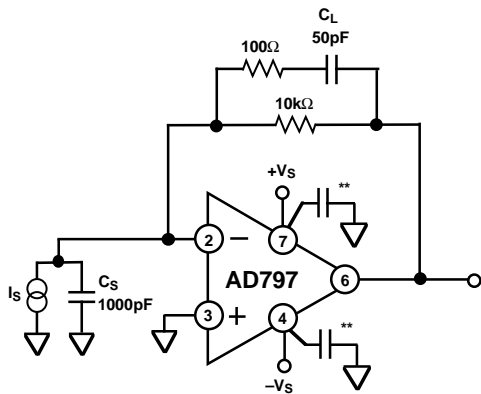


Figure 47. An Ultrasound Preamplifier Circuit

Amorphous (Photodiode) Detector

Large area photodiodes $C_S \geq 500$ pF and certain image detectors (amorphous Si), have optimum performance when used in conjunction with amplifiers with very low voltage rather than very low current noise. Figure 48 shows the AD797 used with an amorphous Si ($C_S = 1000$ pF) detector. The response is adjusted for flatness using capacitor C_L , while the noise is dominated by voltage noise amplified by the ac noise gain. The 797's excellent input noise performance gives 27 μV rms total noise in a 1 MHz bandwidth, as shown by Figure 49.



** USE POWER SUPPLY BYPASSING SHOWN IN FIGURE 32.

Figure 48. Amorphous Detector Preamp

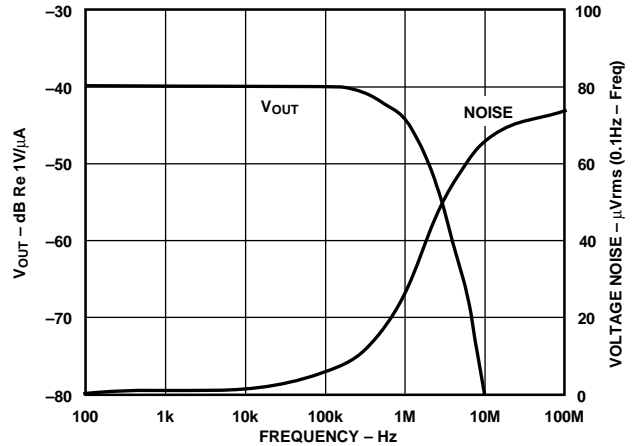
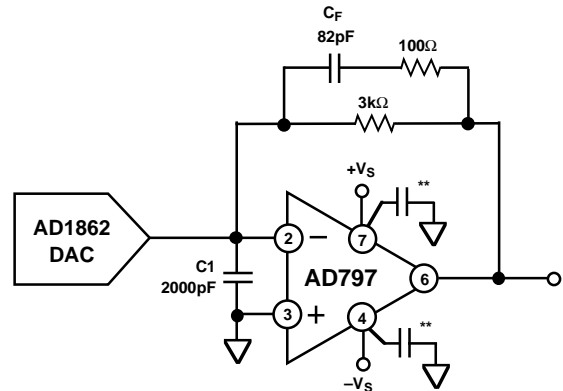


Figure 49. Total Integrated Voltage Noise & V_{OUT} of Amorphous Detector Preamp

Professional Audio Signal Processing—DAC Buffers

The low noise and low distortion of the AD797 make it an ideal choice for professional audio signal processing. An ideal I-to-V converter for a current output DAC would simply be a resistor to ground, were it not for the fact that most DACs do not operate linearly with voltage on their output. Standard practice is to operate an op amp as an I-to-V converter creating a virtual ground at its inverting input. Normally, clock energy and current steps must be absorbed by the op amp's output stage. However, in the configuration of Figure 50, Capacitor C_F shunts high frequency energy to ground, while correctly reproducing the desired output with extremely low THD and IMD.



** USE POWER SUPPLY BYPASSING SHOWN IN FIGURE 32.

Figure 50. A Professional Audio DAC Buffer

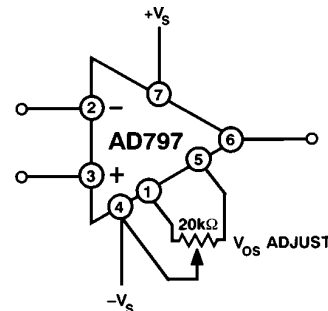
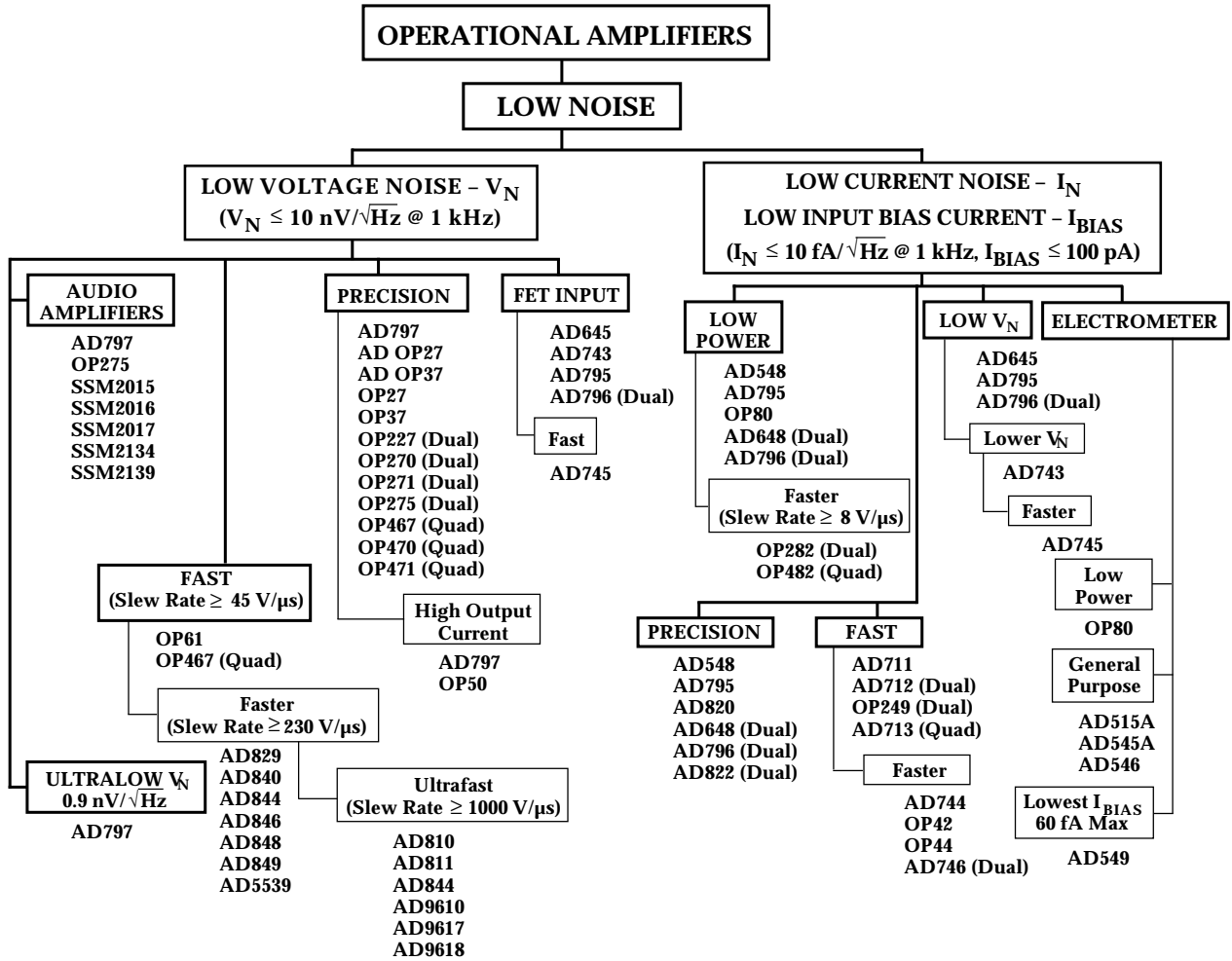
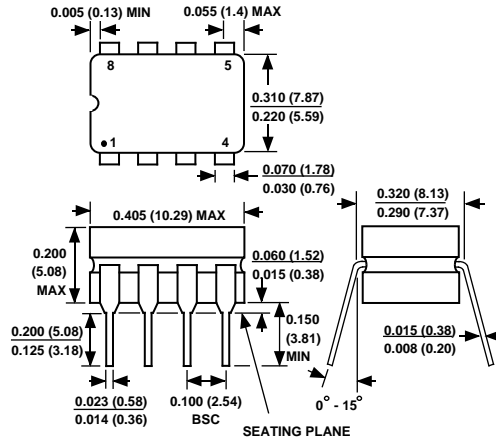


Figure 51. Offset Null Configuration

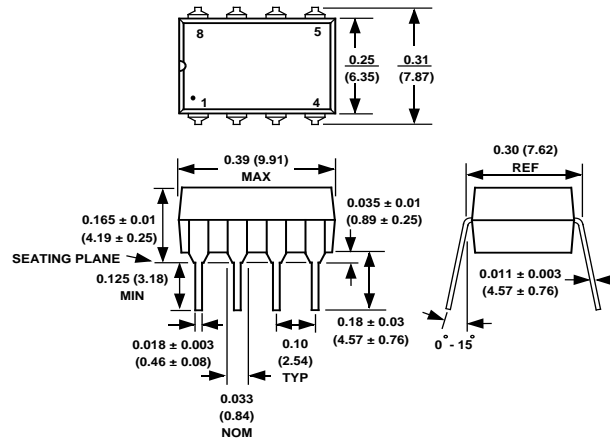


OUTLINE DIMENSIONS
Dimensions shown in inches and (mm).

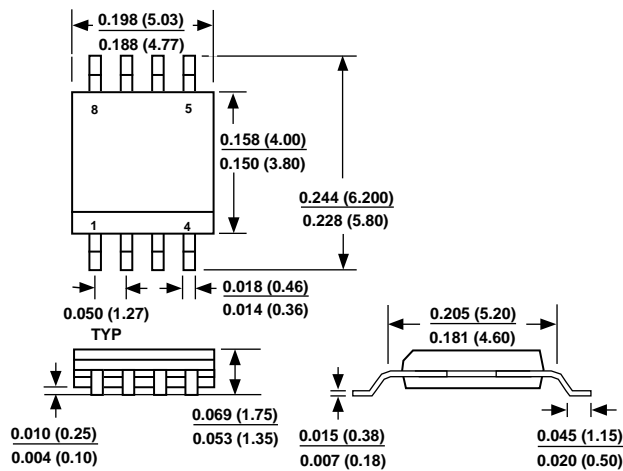
Cerdip (Q) Package*



Plastic Mini-DIP (N) Package



8-Pin SOIC (R) Package



*See military data sheet for 883B specifications.

This datasheet has been download from:

www.datasheetcatalog.com

Datasheets for electronics components.